

GL4A1/GL5A1 Logic Schematics

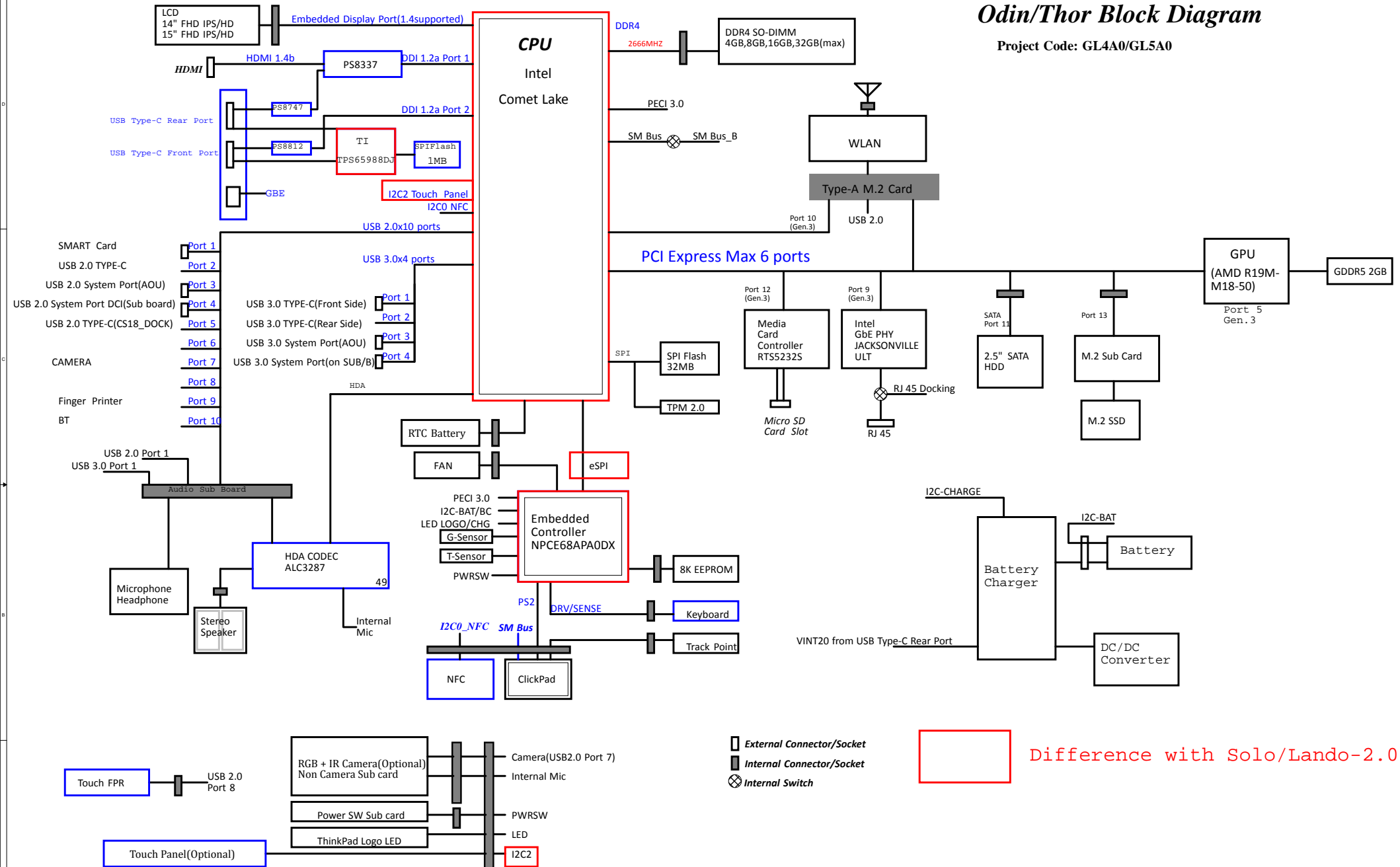
NM-C632

VER 1.0
Feb.12.2020

1.TITLE PAGE	36.DDR4 SUB CHANNEL-B	71.BLANK	106.DC/DC VCC1R2A(SY8310RAC)
2.BLOCK DIAGRAM	37.R19M-M25(1/6) PEG I/F	72.Smart Card Reader	107.DC/DC VCC2R5A(RT8068A)
3.CPU (1/16): DDI/TYPE-C	38.R19M-M25(2/6)_VRAM I/F	73.GBE JACKSONVILLE	108.DC/DC IMVP8(RT3605BE)
4.CPU (2/16): DDR (1/2)	39.BLANK	74.GBE LAN SWITCH	109.DC/DC VCCCPUCORE (RT9610CGQ)
5.CPU (3/16): DDR (2/2)	40.R19M-M25(3/6)DIGITA / XTAL	75.LAN_B CONNECTOR	110.DC/DC VCCGFXCORE_I (RT9610)
6.CPU (4/16): MISC/JTAG	41.R19M-M25(4/6) STRAP / GPIO	76.MEDIA CARD CONTROLLER	111.DC/DC VCCSA (RT9610CGQW)
7.CPU (5/16): ESPI/SPI/SMBUS/C-LINK	42.R19M-M25(5/6) POWER	77.MEDIA CONNECTOR	112.DC/DC Decoupling Cap
8.CPU (6/16): LPSS/ISH	43.BLANK	78.AUDIO ALC3287	113.BLANK
9.CPU (7/16): AUDIO/SDXC	44.R19M-M25(6/6) GND	79.AUDIO CONNECTOR	114.DC/DC VCC1R05_SUS(NB693)
10.CPU (8/16): PCIE/USB/SATA	45.VRAM CHANNEL-A	80.AUDIO JACK SENSE	115.BLANK
11.CPU (9/16): CSI-2/EMMC/CNVI	46.BLANK	81.AUDIO EXT MIC I/F	116.DC/DC VCC1R8_SUS(RT8068A)
12.CPU (10/16): CLOCK SIGNALS	47.BLANK	82.AUDIO SPEAKER	117.BLANK
13.CPU (11/16): SYSTEM PM	48.BLANK	83.AUDIO BEEP	118.DC/DC VCCGFXCORE_D(RT3662EB)
14.CPU (12/16): CPU POWER (1/2)	49.BLANK	84.AUDIO DEBUG	119.BLANK
15.CPU (13/16): CPU POWER (2/2)	50.Load SW VGA	85.EC_NPCE68APA0DX(1/2)	120.DC/DC VCC1R35VIDEO(NB691GG)
16.CPU (14/16): PCH POWER	51.LCD CAMERA/MIC/TOUCH	86.EC_NPCE68APA0DX(2/2)	121.BLANK
17.CPU (15/16): GND	52.Video	87.BLANK	122.BLANK
18.CPU (16/16): CFG/RESERVED	53.BLANK	88.KEYBOARD/TRACK POINT	123.LOADSW VCCIO&VCCST&VCCSTG
19.BLANK	54.HDMI CONNECTOR	89.TOUCH PAD/NFC/FPR	124.LOAD SW PCH SUS
20.RTC BATTERY	55.BLANK	90.FAN CONNECTOR	125.BLANK
21.SPI FLASH	56.BLANK	91.APS G-SENSOR	126.LOAD SW LAN
22.BLANK	57.PCIE Re-driver-1	92.THERMAL SENSOR	127.LOAD SW B
23.BLANK	58.PCIE Re-driver-2	93.SMBUS SWITCH	128.LOAD SW WLAN
24.BLANK	59.THUNDERBOLT PD(TPS65988DJ)	94.BLANK	129.PLM BOM
25.BLANK	60.TUNDERBOLT PD(BLANK)	95.BLANK	
26.BLANK	61.USB TYPE-C SWITCH	96.SATA HDD CONN	
27.BLANK	62.DOCKING CONNECTOR	97.SATA Re-driver	
28.BLANK	63.TYPE-C CONNECTOR	98.DISCRETE TPM 2.0	
29.BLANK	64.M.2 SOCKET 3 MODULE I/F	99.SCREW HOLES	
30.BLANK	65.BLANK	100.DC-IN	
31.BLANK	66.WLAN	101.BATTERY INPUT	
32.BLANK	67.M.2 SOCKET	102.BATTERY CHARGER(BQ25700A)	
33.DDR4 SUB CHANNEL-A	68.DDI DEMULTIPLEXER	103.DC/DC VCC5M (LV6228C)	
34.DDR4 SUB CHANNEL-A	69.USB TYPE-A CONNECTOR	104.DC/DC +5VTPC(LV6228C)	
35.DDR4 SUB CHANNEL-B	70.USB TYPE-A CONN	105.DC/DC VCC3M (SYX198B)	

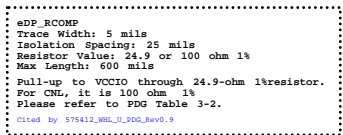
Odin/Thor Block Diagram

Project Code: GL4A0/GL5A0



GPP_E19/DDP1_CTRLDATA/TBT_LX0_RXD (DDP1 I2C / TBT LX#0 PINS VCCIO CONFIGURATION)	
GPP_E21/DDP2_CTRLDATA/TBT_LX1_RXD (DDP2 I2C / TBT LX#1 PINS VCCIO CONFIGURATION)	
GPP_D10/DDP3_CTRLDATA/TBT_LX2_RXD (DDP3 I2C / TBT LX#2 PINS VCCIO CONFIGURATION)	
GPP_D12/DDP4_CTRLDATA/TBT_LX3_RXD (DDP4 I2C / TBT LX#3 PINS VCCIO CONFIGURATION)	
HIGH	3.3V
LOW	1.8V

DP port	Enable	Disable
DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm \pm 5% resistor	no connect
DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm \pm 5% resistor	no connect



VCC1R2A VCC1R2A 5,15,33,34,35,36,106
VCC3M VCC3M 11,13,15,16,50,51,59,78,84,85,86,88,102,103,104,105,106,114,123,124,126,127,128

TABLE

Pin	Interleave	Non-Interleave
AL71	DDR0_DQ[0]	DDR0_DQ[0]
AL68	DDR0_DQ[1]	DDR0_DQ[1]
AN68	DDR0_DQ[2]	DDR0_DQ[2]
AN69	DDR0_DQ[3]	DDR0_DQ[3]
AL70	DDR0_DQ[4]	DDR0_DQ[4]
AL69	DDR0_DQ[5]	DDR0_DQ[5]
AN70	DDR0_DQ[6]	DDR0_DQ[6]
AN71	DDR0_DQ[7]	DDR0_DQ[7]
AR68	DDR0_DQ[8]	DDR0_DQ[8]
AU71	DDR0_DQ[9]	DDR0_DQ[9]
AU68	DDR0_DQ[10]	DDR0_DQ[10]
AR71	DDR0_DQ[11]	DDR0_DQ[11]
AR69	DDR0_DQ[12]	DDR0_DQ[12]
AU70	DDR0_DQ[13]	DDR0_DQ[13]
AU69	DDR0_DQ[14]	DDR0_DQ[14]
	DDR0_DQ[15]	DDR0_DQ[15]

BB65	DDR0_DQ[16]	DDR0_DQ[32]
AW65	DDR0_DQ[17]	DDR0_DQ[33]
AW63	DDR0_DQ[18]	DDR0_DQ[34]
AY63	DDR0_DQ[19]	DDR0_DQ[35]
BA65	DDR0_DQ[20]	DDR0_DQ[36]
AY65	DDR0_DQ[21]	DDR0_DQ[37]
BA63	DDR0_DQ[22]	DDR0_DQ[38]
BB63	DDR0_DQ[23]	DDR0_DQ[39]
BA61	DDR0_DQ[24]	DDR0_DQ[40]
AW61	DDR0_DQ[25]	DDR0_DQ[41]
BB59	DDR0_DQ[26]	DDR0_DQ[42]
AW59	DDR0_DQ[27]	DDR0_DQ[43]
BB61	DDR0_DQ[28]	DDR0_DQ[44]
AY61	DDR0_DQ[29]	DDR0_DQ[45]
BA59	DDR0_DQ[30]	DDR0_DQ[46]
AY59	DDR0_DQ[31]	DDR0_DQ[47]

AY39	DDR0_DQ[32]	DDR1_DQ[0]
AW39	DDR0_DQ[33]	DDR1_DQ[1]
AY37	DDR0_DQ[34]	DDR1_DQ[2]
AW37	DDR0_DQ[35]	DDR1_DQ[3]
BB39	DDR0_DQ[36]	DDR1_DQ[4]
BA39	DDR0_DQ[37]	DDR1_DQ[5]
EA37	DDR0_DQ[38]	DDR1_DQ[6]
BB37	DDR0_DQ[39]	DDR1_DQ[7]
AY35	DDR0_DQ[40]	DDR1_DQ[8]
AW35	DDR0_DQ[41]	DDR1_DQ[9]
AY33	DDR0_DQ[42]	DDR1_DQ[10]
AW33	DDR0_DQ[43]	DDR1_DQ[11]
BB35	DDR0_DQ[44]	DDR1_DQ[12]
BA35	DDR0_DQ[45]	DDR1_DQ[13]
BA33	DDR0_DQ[46]	DDR1_DQ[14]
BB33	DDR0_DQ[47]	DDR1_DQ[15]

AY31	DDR0_DQ[48]	DDR1_DQ[32]
AW31	DDR0_DQ[49]	DDR1_DQ[33]
AY29	DDR0_DQ[50]	DDR1_DQ[34]
AW29	DDR0_DQ[51]	DDR1_DQ[35]
BB31	DDR0_DQ[52]	DDR1_DQ[36]
BA31	DDR0_DQ[53]	DDR1_DQ[37]
BA29	DDR0_DQ[54]	DDR1_DQ[38]
BB29	DDR0_DQ[55]	DDR1_DQ[39]
AY27	DDR0_DQ[56]	DDR1_DQ[40]
AW27	DDR0_DQ[57]	DDR1_DQ[41]
AY25	DDR0_DQ[58]	DDR1_DQ[42]
AW25	DDR0_DQ[59]	DDR1_DQ[43]
BB27	DDR0_DQ[60]	DDR1_DQ[44]
BA25	DDR0_DQ[61]	DDR1_DQ[45]
BB25	DDR0_DQ[62]	DDR1_DQ[46]
	DDR0_DQ[63]	DDR1_DQ[47]

LOGIC

M_A_DQ0	A26	DDR0_DQ[0]	DDR0_DQ[0]
M_A_DQ1	D26	DDR0_DQ[1]	DDR0_DQ[1]
M_A_DQ2	D28	DDR0_DQ[2]	DDR0_DQ[2]
M_A_DQ3	C26	DDR0_DQ[3]	DDR0_DQ[3]
M_A_DQ4	B26	DDR0_DQ[4]	DDR0_DQ[4]
M_A_DQ5	C28	DDR0_DQ[5]	DDR0_DQ[5]
M_A_DQ6	B28	DDR0_DQ[6]	DDR0_DQ[6]
M_A_DQ7	A28	DDR0_DQ[7]	DDR0_DQ[7]
M_A_DQ8	D30	DDR0_DQ[8]	DDR0_DQ[8]
M_A_DQ9	C30	DDR0_DQ[9]	DDR0_DQ[9]
M_A_DQ10	B30	DDR0_DQ[10]	DDR0_DQ[10]
M_A_DQ11	A30	DDR0_DQ[11]	DDR0_DQ[11]
M_A_DQ12	D32	DDR0_DQ[12]	DDR0_DQ[12]
M_A_DQ13	C32	DDR0_DQ[13]	DDR0_DQ[13]
M_A_DQ14	B32	DDR0_DQ[14]	DDR0_DQ[14]
M_A_DQ15	A32	DDR0_DQ[15]	DDR0_DQ[15]
M_A_DQ16	D34	DDR0_DQ[16]	DDR0_DQ[16]
M_A_DQ17	C34	DDR0_DQ[17]	DDR0_DQ[17]
M_A_DQ18	B34	DDR0_DQ[18]	DDR0_DQ[18]
M_A_DQ19	A34	DDR0_DQ[19]	DDR0_DQ[19]
M_A_DQ20	D36	DDR0_DQ[20]	DDR0_DQ[20]
M_A_DQ21	C36	DDR0_DQ[21]	DDR0_DQ[21]
M_A_DQ22	B36	DDR0_DQ[22]	DDR0_DQ[22]
M_A_DQ23	A36	DDR0_DQ[23]	DDR0_DQ[23]
M_A_DQ24	D38	DDR0_DQ[24]	DDR0_DQ[24]
M_A_DQ25	C38	DDR0_DQ[25]	DDR0_DQ[25]
M_A_DQ26	B38	DDR0_DQ[26]	DDR0_DQ[26]
M_A_DQ27	A38	DDR0_DQ[27]	DDR0_DQ[27]
M_A_DQ28	D40	DDR0_DQ[28]	DDR0_DQ[28]
M_A_DQ29	C40	DDR0_DQ[29]	DDR0_DQ[29]
M_A_DQ30	B40	DDR0_DQ[30]	DDR0_DQ[30]
M_A_DQ31	A40	DDR0_DQ[31]	DDR0_DQ[31]
M_A_DQ32	D42	DDR0_DQ[32]	DDR0_DQ[32]
M_A_DQ33	C42	DDR0_DQ[33]	DDR0_DQ[33]
M_A_DQ34	B42	DDR0_DQ[34]	DDR0_DQ[34]
M_A_DQ35	A42	DDR0_DQ[35]	DDR0_DQ[35]
M_A_DQ36	D44	DDR0_DQ[36]	DDR0_DQ[36]
M_A_DQ37	C44	DDR0_DQ[37]	DDR0_DQ[37]
M_A_DQ38	B44	DDR0_DQ[38]	DDR0_DQ[38]
M_A_DQ39	A44	DDR0_DQ[39]	DDR0_DQ[39]
M_A_DQ40	D46	DDR0_DQ[40]	DDR0_DQ[40]
M_A_DQ41	C46	DDR0_DQ[41]	DDR0_DQ[41]
M_A_DQ42	B46	DDR0_DQ[42]	DDR0_DQ[42]
M_A_DQ43	A46	DDR0_DQ[43]	DDR0_DQ[43]
M_A_DQ44	D48	DDR0_DQ[44]	DDR0_DQ[44]
M_A_DQ45	C48	DDR0_DQ[45]	DDR0_DQ[45]
M_A_DQ46	B48	DDR0_DQ[46]	DDR0_DQ[46]
M_A_DQ47	A48	DDR0_DQ[47]	DDR0_DQ[47]

TABLE

Pin	Interleave	Non-Interleave
AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
AT70	DDR0_DQSP[1]	DDR0_DQSP[1]

BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
BA60	DDR0_DQSP[3]	DDR0_DQSP[5]

BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
BA34	DDR0_DQSP[5]	DDR1_DQSP[1]

BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

LOGIC

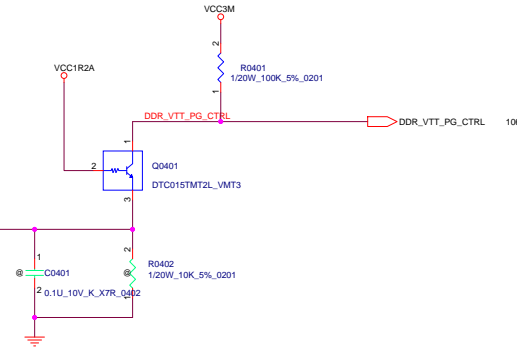
TABLE

Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]

AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[11]	DDR0_CAB[8]	DDR0_MA[11]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

LOGIC

Vendor	LCFC P/N	Description
ROHM	SB00000WC0J	S TR DTC015MT2L NPN VMT3
TOSHIBA	SB000010700	S TR RN1131MFV NPN VESM
ON	SB000013J00	S TR DTC115T3T5G NPN SOT-723-



LOGIC



[WHL PDG]for CNL DDR4 COMPENSATION
DDR_RCOMP[0] Pull down 100 ohm resistor
DDR_RCOMP[1] Pull down 100 ohm resistor
DDR_RCOMP[2] Pull down 100 ohm resistor

LOGIC

Table 3-2. RCOMP Recommendation for CNL

LOGIC

Rev
1.0

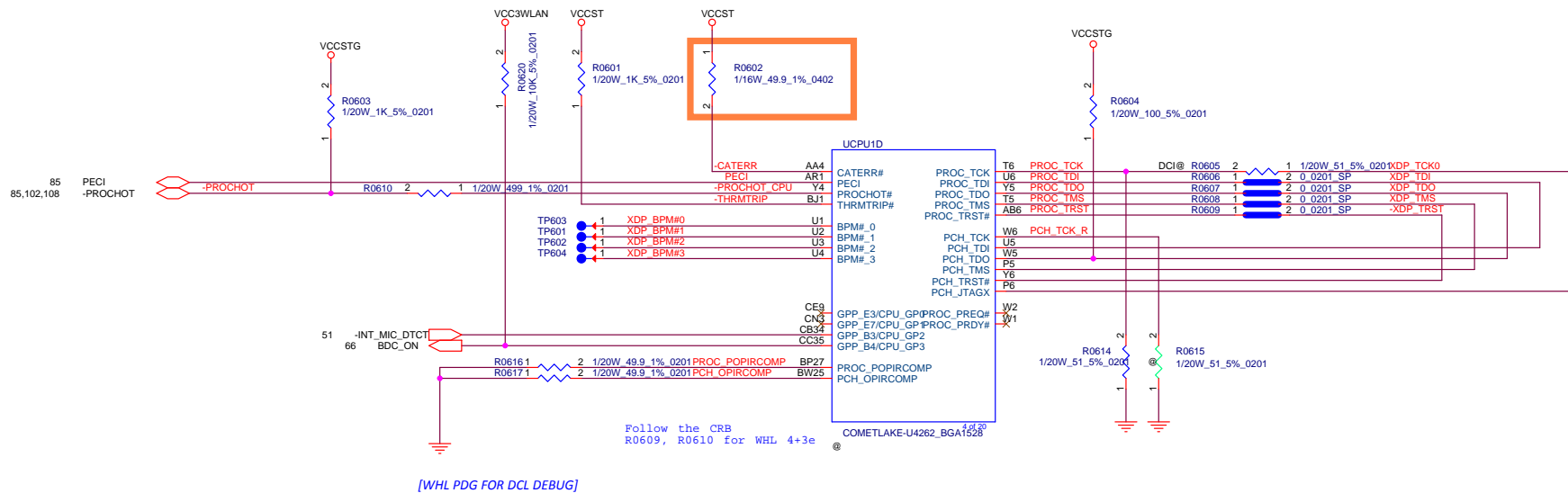
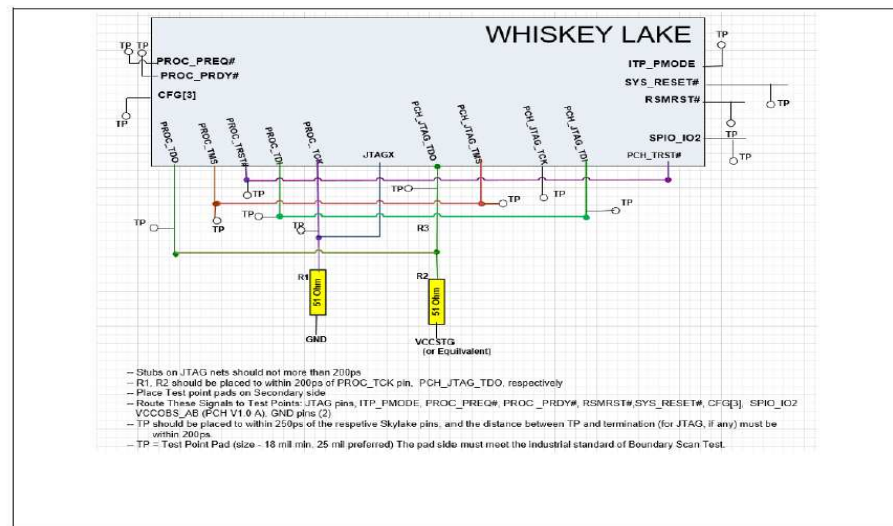
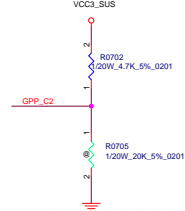
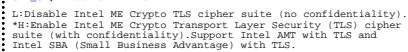
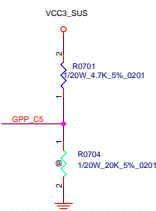
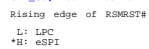


Figure 13-6. Primary Debug Portconnector Less Routing Topology

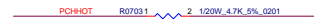


Security Classification			
LC Future Center Secret Data			
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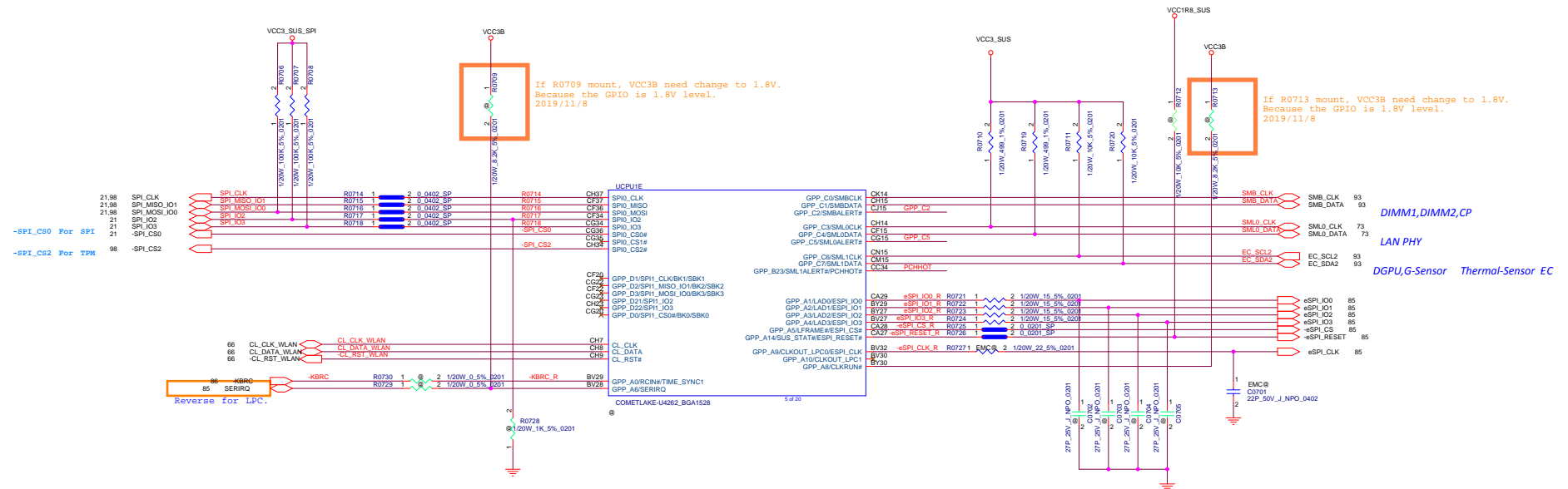
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WHL(D)_MISC/ JTAG			
Size	Document Number	Rev	1.0
Custom	GLAA1/GL5A1 NM-C632		
Date:	Tuesday, March 03, 2020	Sheet	6 of 128



This signal has an internal pull-down.
0 = Disable Intel® DCI-OOB (Default)
1 = Enable Intel® DCI-OOB

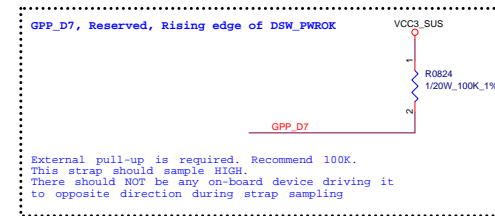


SP10_M051	Reserved	Rising edge of RSMS1#	External pull-up is required. Recommended 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it at opposite direction during strap sampling.
SP10_I02	Reserved	Rising edge of RSMS1#	External pull-up is required. Recommended 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it at opposite direction during strap sampling.
SP10_I03	Reserved	Rising edge of RSMS1#	External pull-up is required. Recommended 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it at opposite direction during strap sampling.



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Issued Date	2015/01/12	Deciphered Date	2016/01/12
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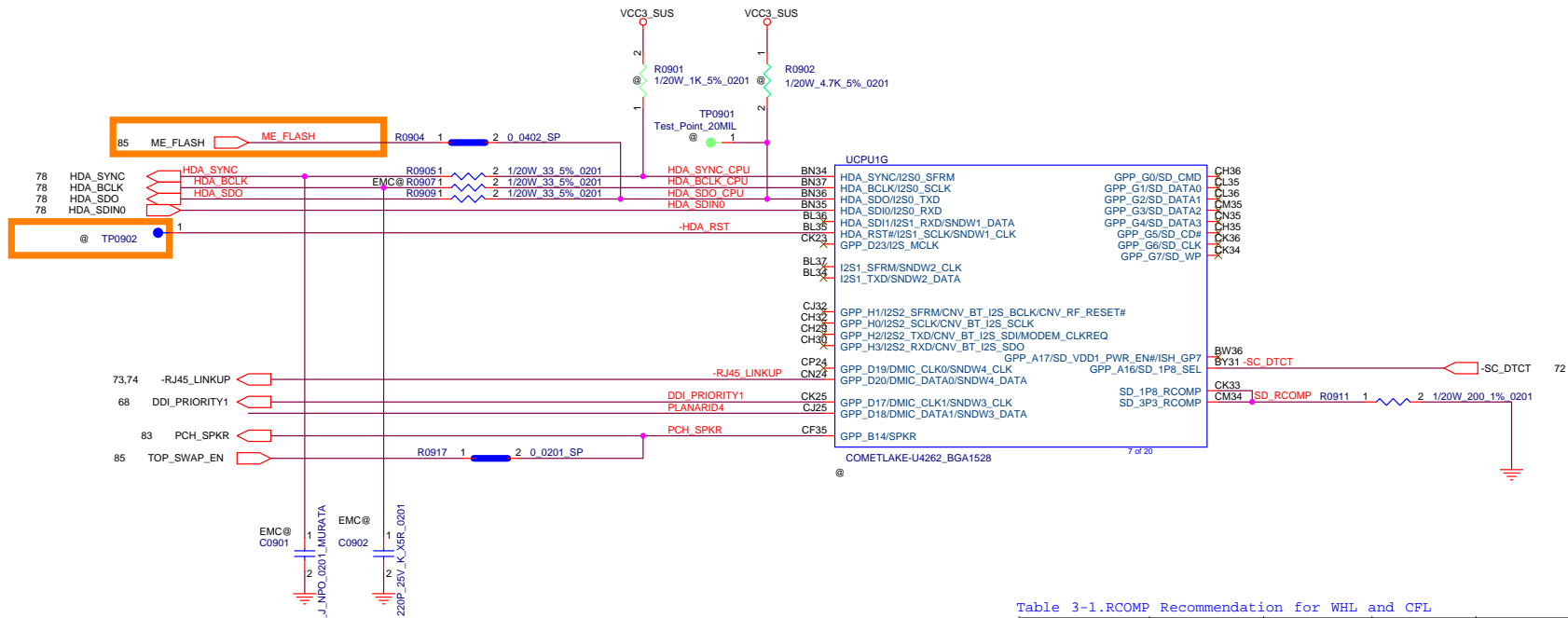
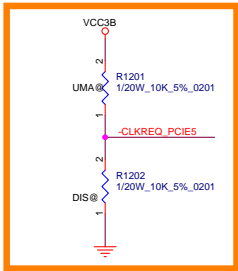


Table 3-1.RCOMP Recommendation for WHL and CFL

SD3 & EMMC	SD_1P8_RCOMP SD_3P3_RCOMP EMMC_RCOMP	200Ω ±1% to GND	<0.1	Notes: These pins can be merged into one 200Ω +/- 1% to GND resistor. Routing each of them to individual 200Ω +/-1% to GND resistor is an option too.
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TPM ID

Status	PLANARID4 (GPP_D18)
TPM	0 (R0913)
NTPM	1 (R0911)



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7.3.2.3 WHLU PCH-LP Platform XTAL Routing Guidelines

Figure 7-7. WHLU PCH-LP Platform Crystal XTAL_IN/OUT Topology

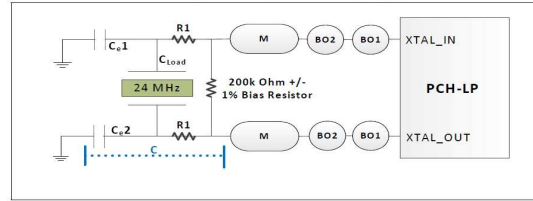


TABLE of (Y1201)		
Vendor	LCFC P/N	Description
TXC	SJ10000S500	S CRYSTAL 24MHZ 12PF +-20PPM 8Y24000034
Harmony	SJ10000RR00	S CRYSTAL 24MHZ 12PF X2C024000DC1H-HU

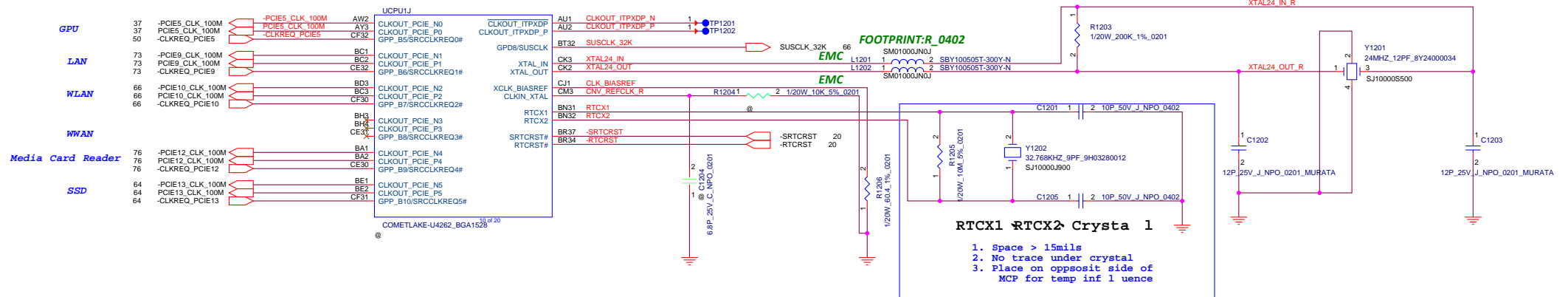

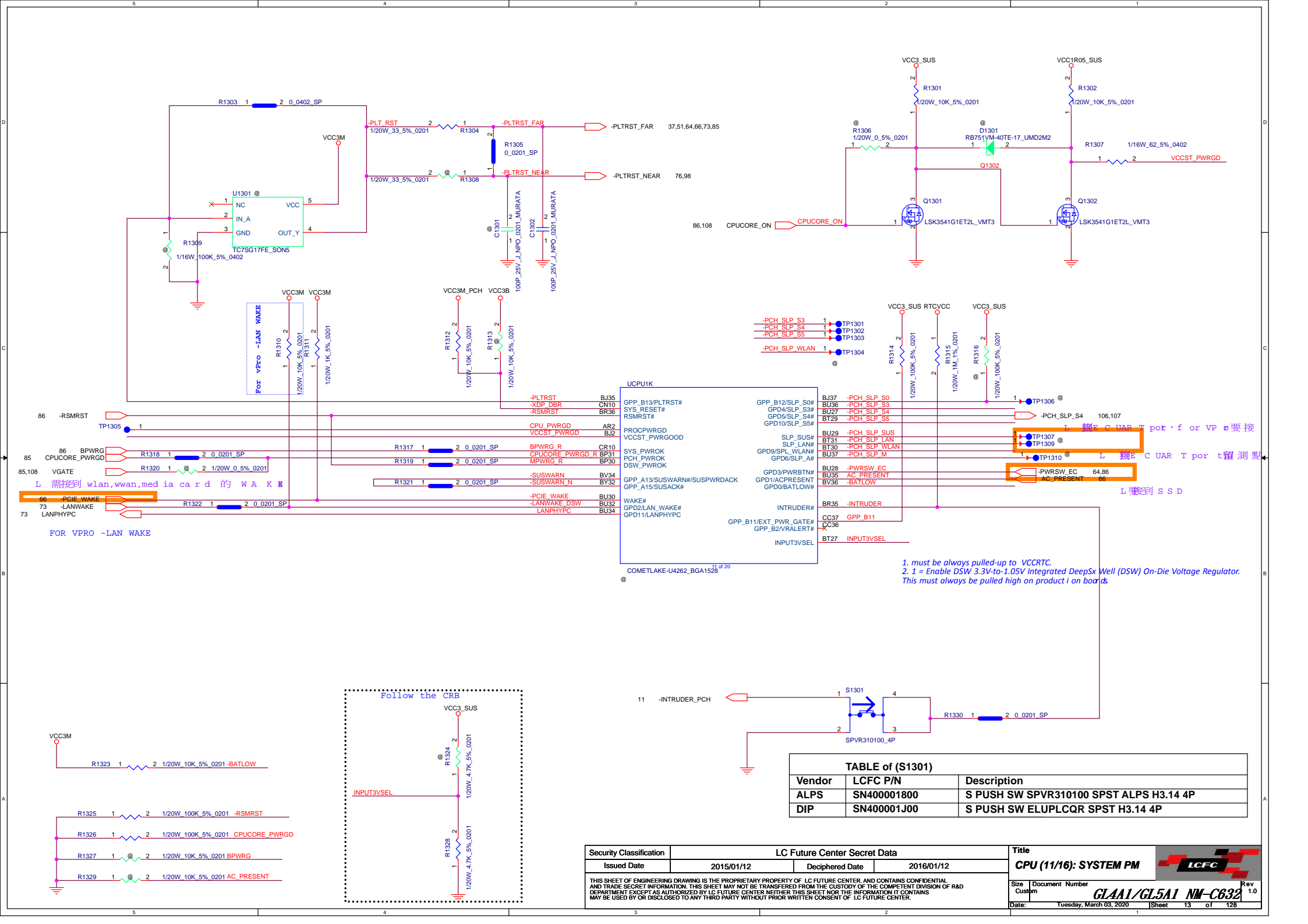
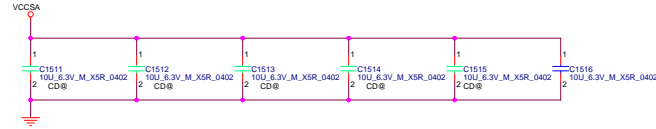


TABLE of XTAL (Y1202)		
Vendor	LCFC P/N	Description
TXC	SJ10000J900	S CRYSTAL 32.768KHZ 9PF 20PPM
KDS	SJ100069400	S CRYSTAL 32.768KHZ 9PF 1TJF09
SEIKO	SJ10000IX00	S CRYSTAL 32.768KHZ 9PF X1A000

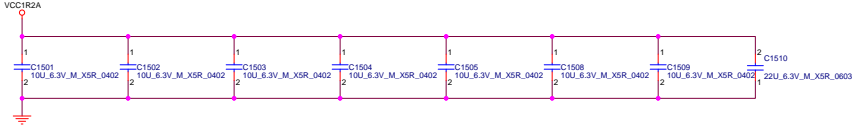
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Date:	Tuesdav. March 03, 2020		Sheet	12	of 128



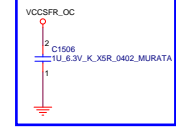
Comet Lake U 4+2 Processor]VCCSA
Comet Lake U 4+2 Processor[BOTTOM]10uF x6 47uF x2



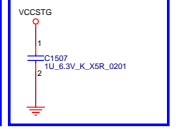
Comet Lake U 4+2 Processor]VDDQ
Comet Lake U 4+2 Processor[BOTTOM]10uF x6, 22uF x1



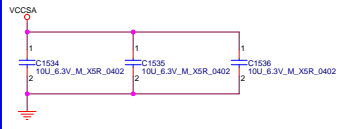
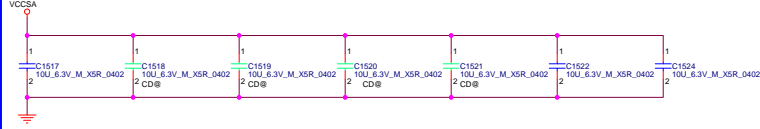
[CML F80]VCCPL1_OC
[CML F80]1uF x1
Primary side cap



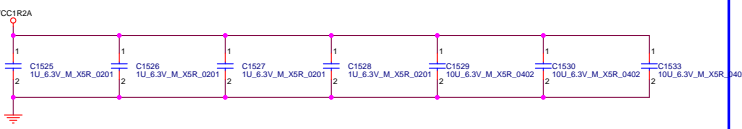
[CML F80]VCCSTG
[CML F80]1uF x1
Primary side cap



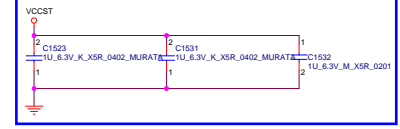
Comet Lake U 4+2 Processor]VCCSA
Comet Lake U 4+2 Processor[TOP]10uF x7



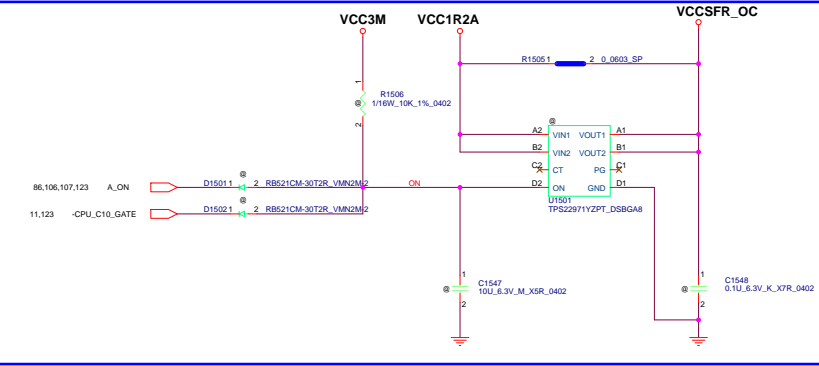
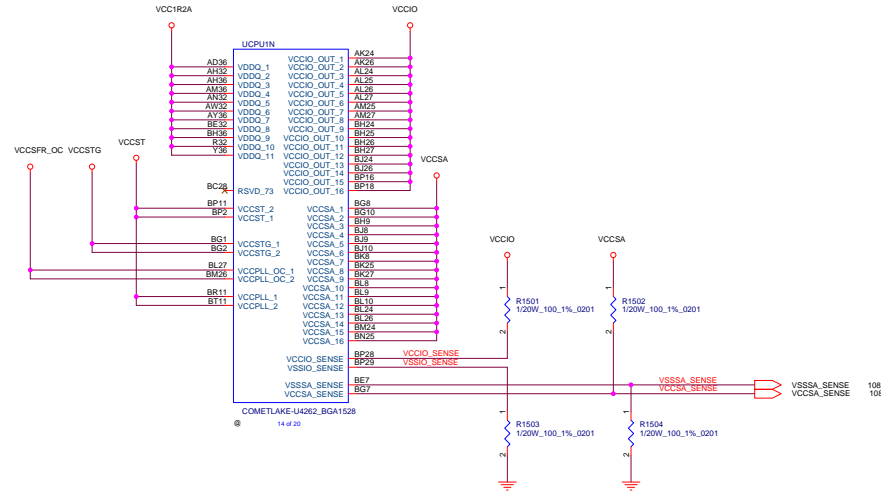
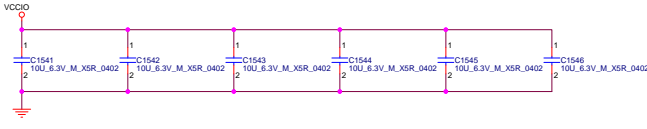
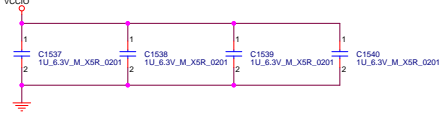
Comet Lake U 4+2 Processor]VDDQ
Comet Lake U 4+2 Processor[TOP]1uF x4, 10uF x3




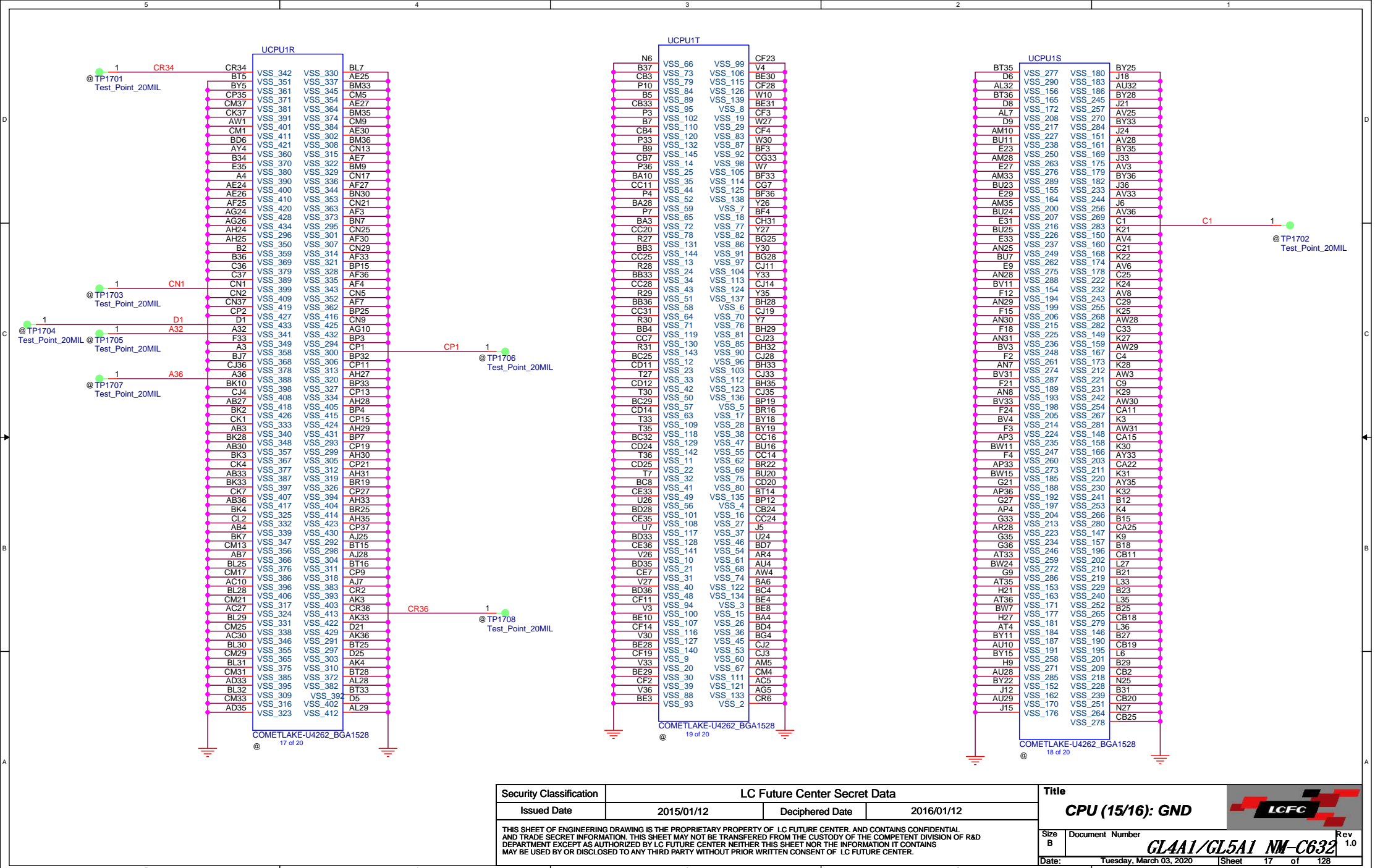
[CML F80]VCCST
[CML F80]1uF x1
Primary side cap




Comet Lake U 4+2 Processor]VCCIO
Comet Lake U 4+2 Processor[BOTTOM]1uF x4, 10uF x6



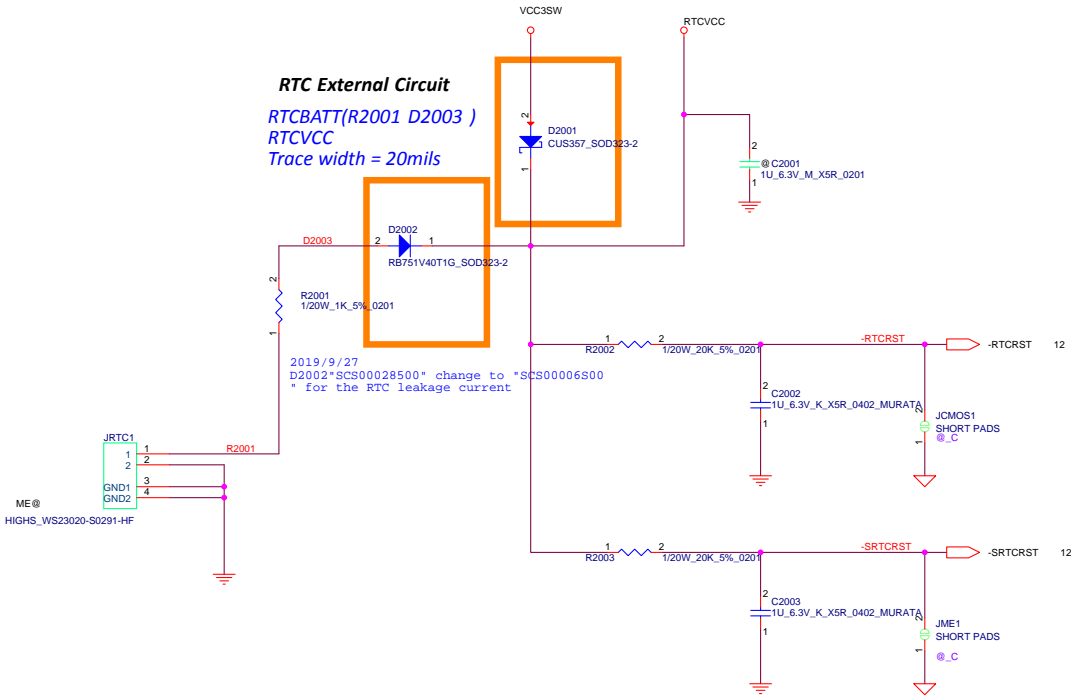
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	CPU (13/16): CPU POWER (2) 	
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RTC CONN.



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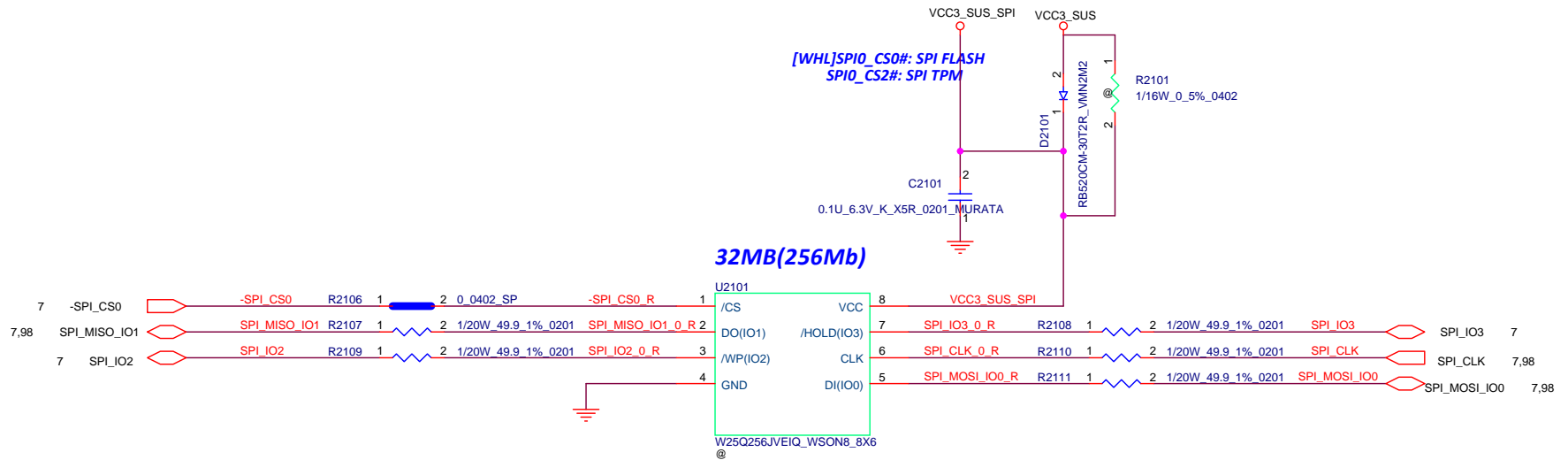


TABLE of SPI ROM (U2102)

Vendor	LCFC P/N	Description
MXIC	SA00008J400	S IC FL 256M MX25L25673GM2I-08G SOP 8P
Winbond	SA00008WZ00	S IC FL 256M W25Q256JVEIQ WSON 8P SPI
GD	SA00009R800	S IC FL 256M GD25B256DYIGR WSON 8P SPI

32MB (256Mb) 200MIL SOIC8
 MACRONIX MX25L25673GM2I-08G
 MACRONIX MX25L25673GM2I-10G


32MB (256Mb) 8x6mm WSON8 (Optional)
 WINBOND W25Q256JVEIQ

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				Date: Tuesday, March 03, 2020	Rev 1.0	Sheet 30 of 128

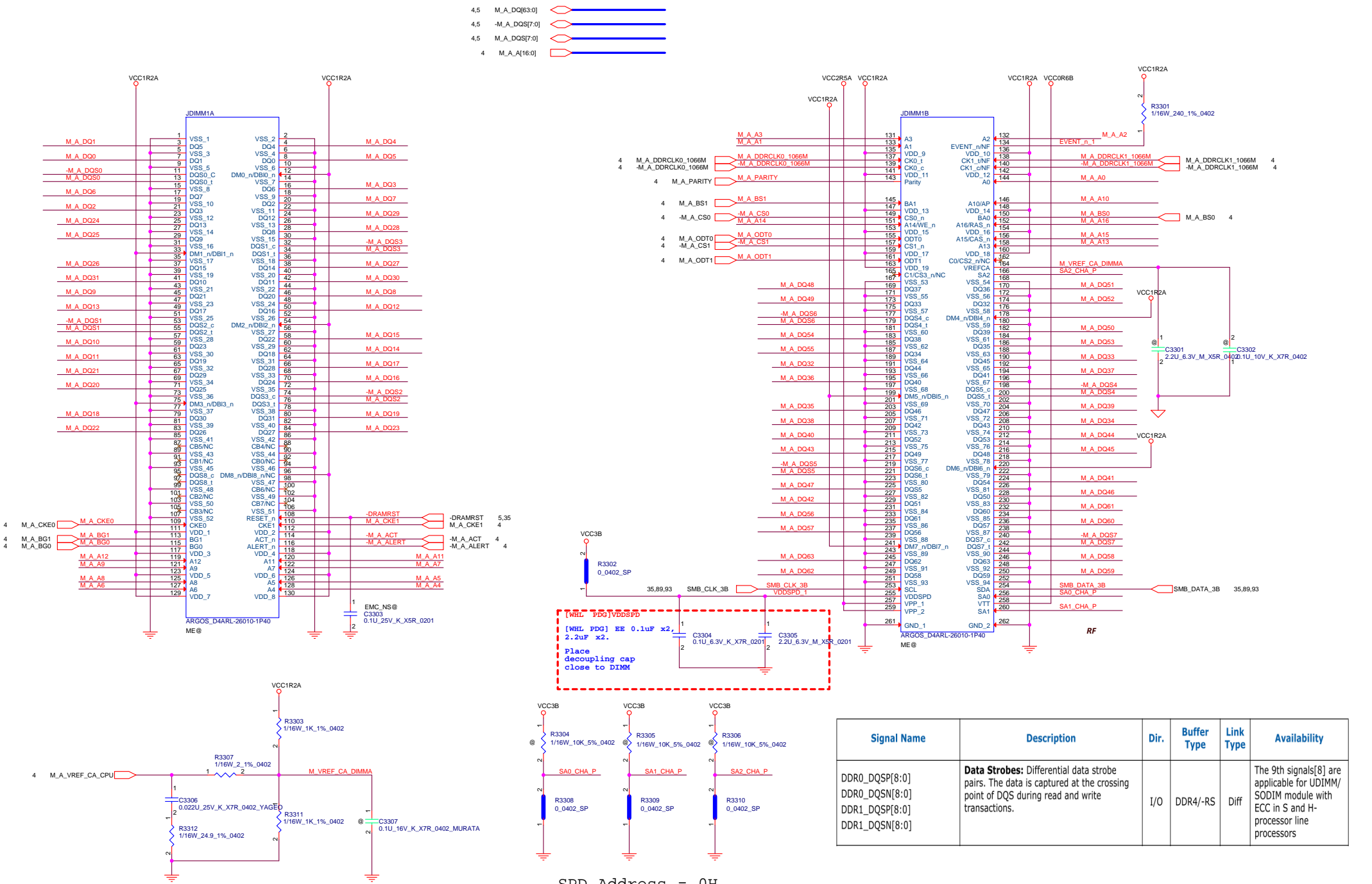
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				Date: Tuesday, March 03, 2020		Rev 1.0
				Sheet 31 of 128		

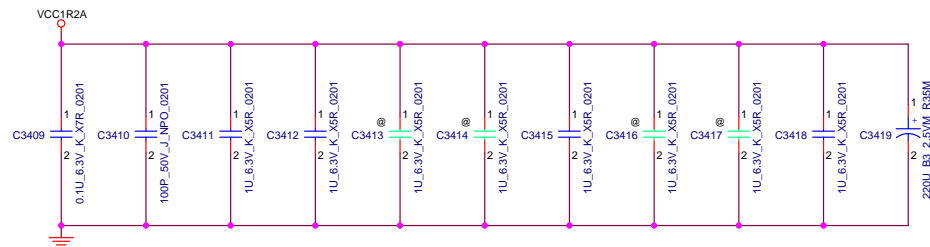
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				Date:	Tuesday, March 03, 2020	Sheet 32 of 128



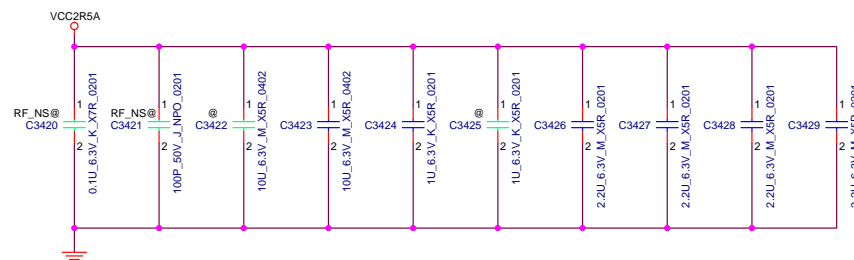
Place 10uF/1uF decoupling cap, 4
near each side of the DIMM
connector close to VDD pins.
330uF placeholder

The schematic shows a power supply rail starting from a VCC1R2A input. The rail is connected to a series of decoupling capacitors, each with a value of 100 nF (labeled as 100_6.3V_M_X5R_0603_YAGEO). The capacitors are labeled C3401 through C3408. The rail is connected to ground at the end.



10U x 6
0.1U x 2
1U x 4
220U x 1

Place decoupling cap on DRAM side.



10U x 1
1U x 1

10U x 1
1U x 2

Place decoupling on the VTT plane close to SODIMM

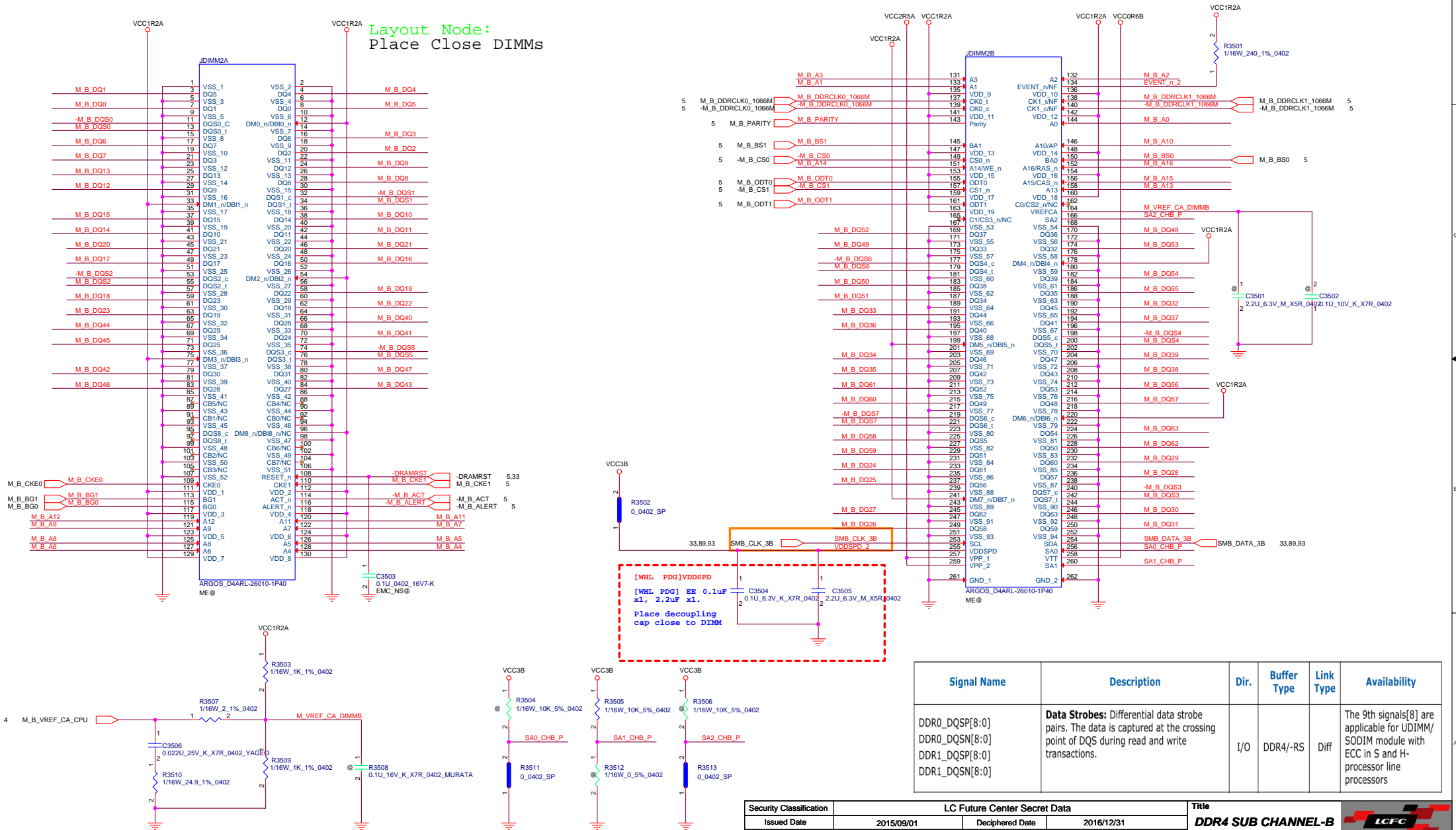
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Total
10U x 8
0.1U x 2
1U x 7
220U x 1

```

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Title			
DDR4 SUB CHANNEL-A			
Size	Document Number	Rev	
Custom	GL4A1/GL5A1 NM-C632	1.0	
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SPD Address = 2H

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-RS	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification

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Deciphered Date

2016/12/31

Title

DDR4 SUB CHANNEL-B

Size

Custom

Document Number

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Date

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Rev

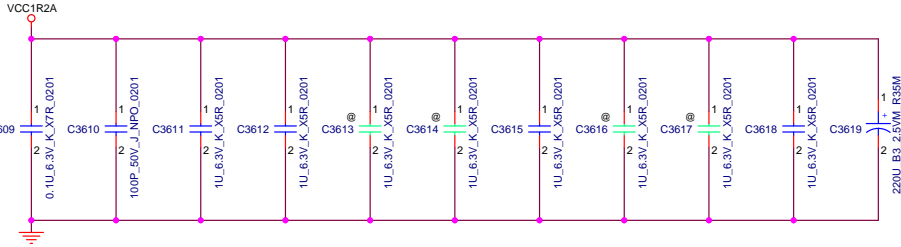
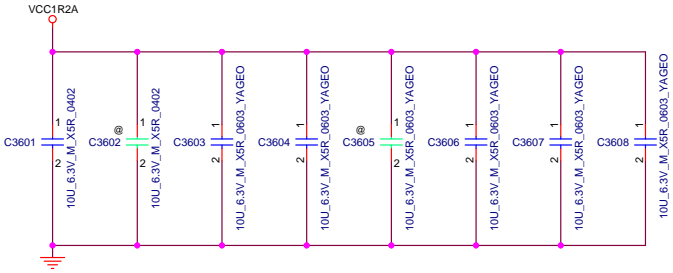
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LCFC

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Place 10uF/1uF decoupling cap, 4
near each side of the DIMM
connector close to VDD pins.
330uF placeholder

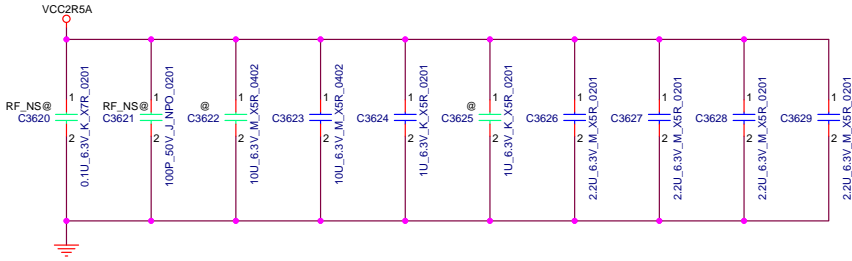
Total quantity is referring to 2 channels.



10U x 6
0.1U x 2
1U x 4
220U x 1

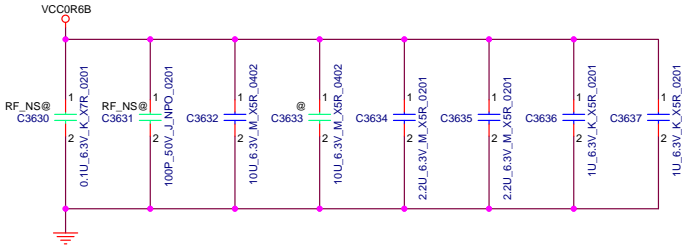
[WHL PDG]VPP
[WHL PDG] EE 10uF x2, 1uF x2.
Place decoupling cap on DRAM side.

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10U x 1
1U x 1

[WHL PDG]VTT
[WHL PDG] EE 10uF x2, 1uF x4.

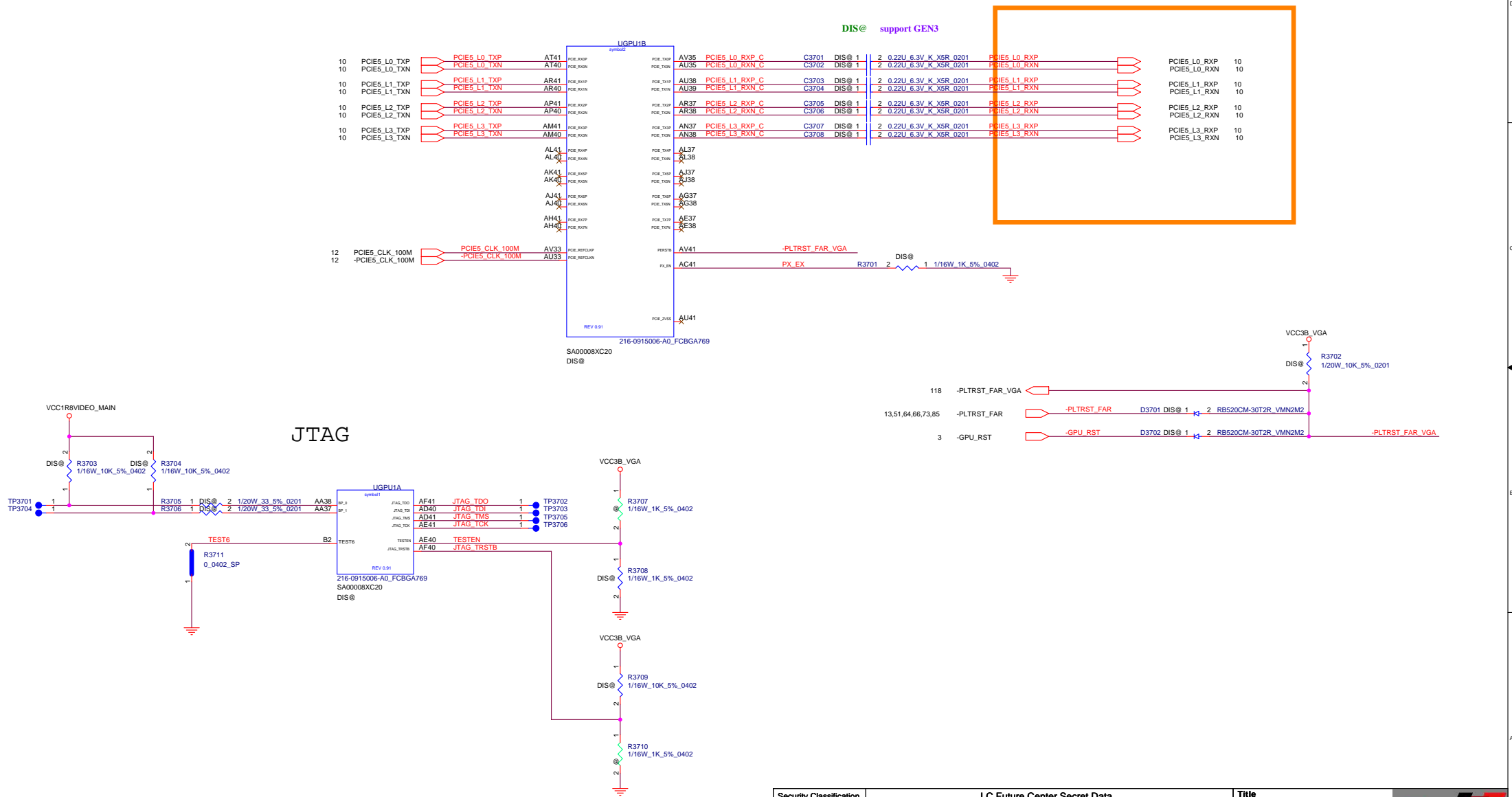



10U x 1
1U x 2

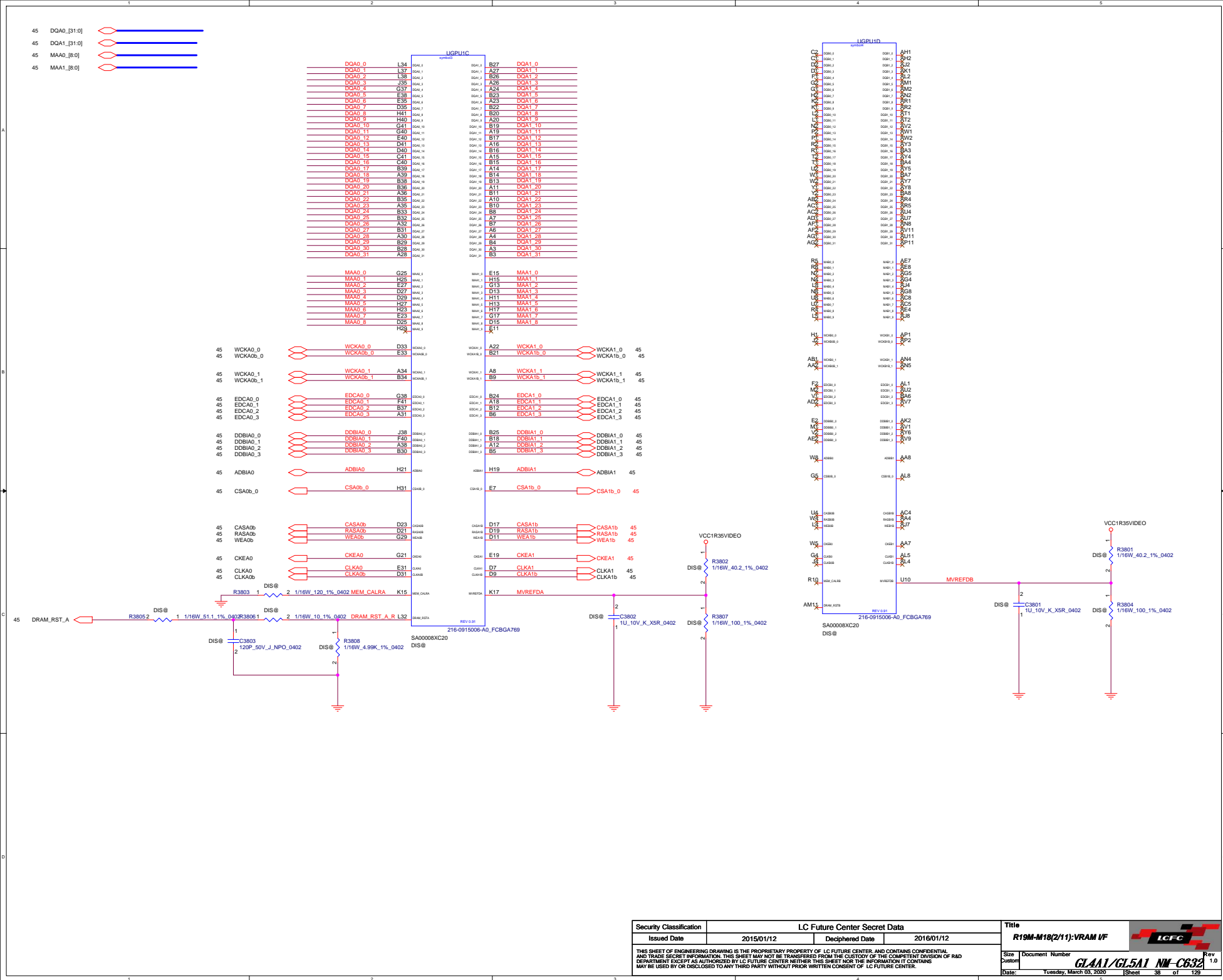
Place decoupling on the VTT plane close to SODIMM

Total
10U x 8
0.1U x 2
1U x 7
220U x 1


TABLE of GPU (UGPU1)		
Vendor	LCFC P/N	Description
AMD(R19M-M18-50)	SA00008XC20	S IC 216-0915006 D1 FCBGA GPU R19M 01 !



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				Date:	Tuesday, March 03, 2020	Rev 1.0
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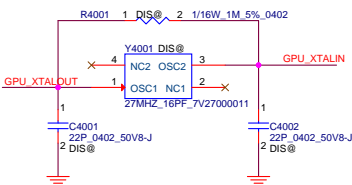
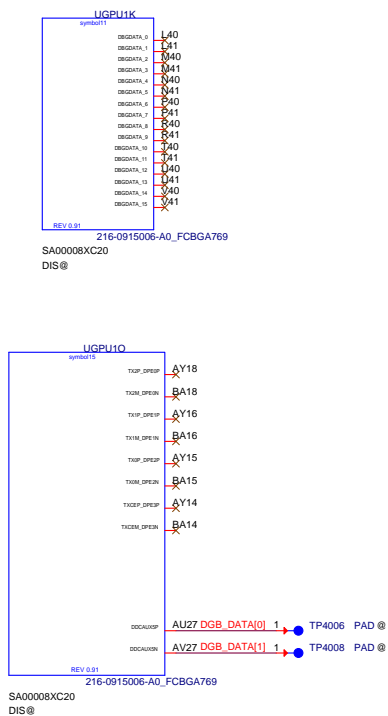
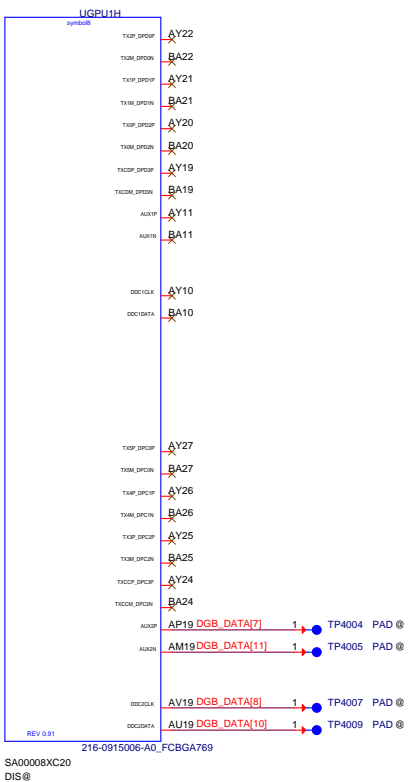
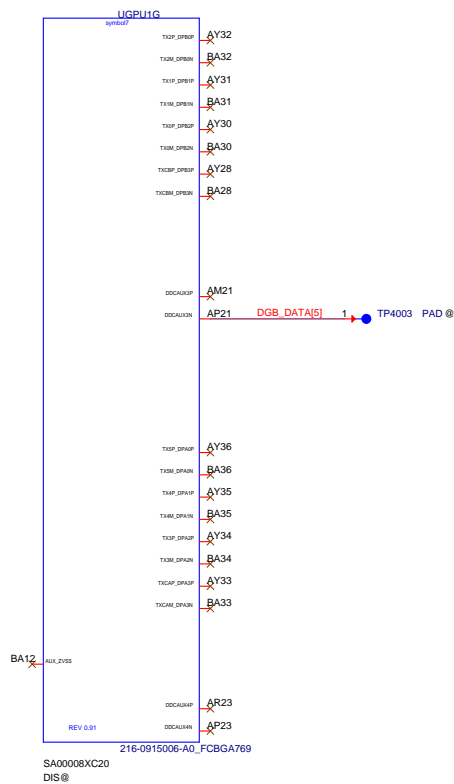

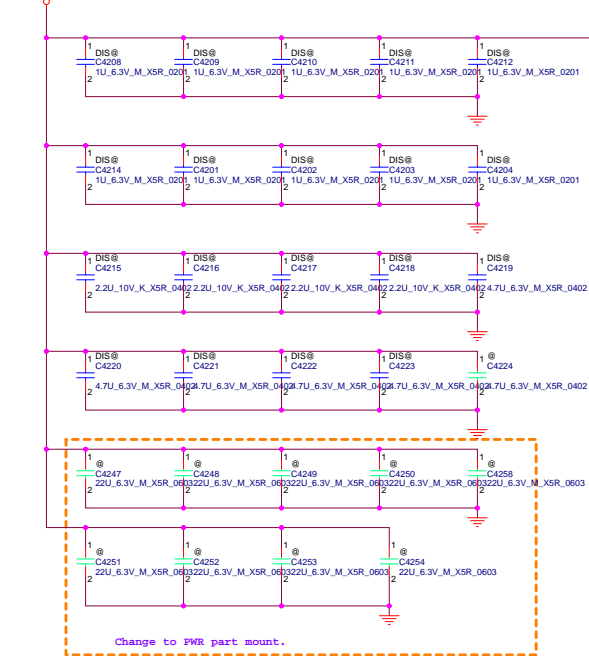


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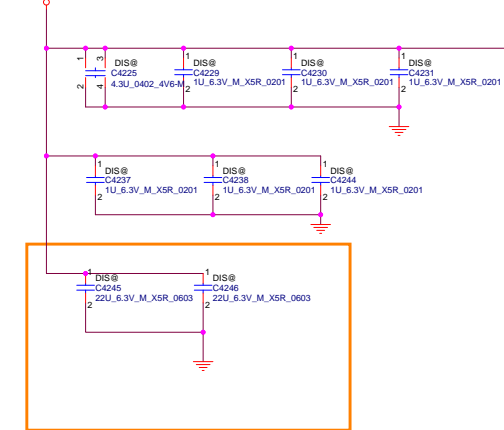


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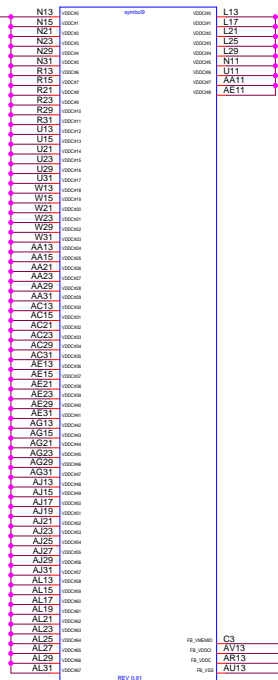
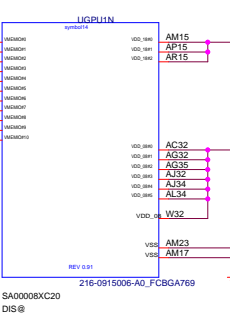
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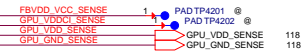
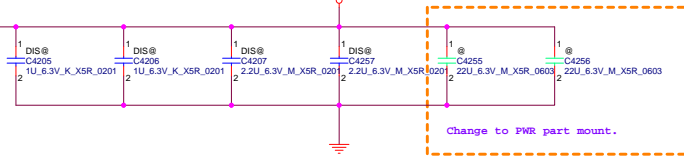
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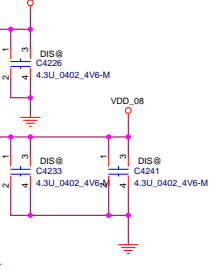
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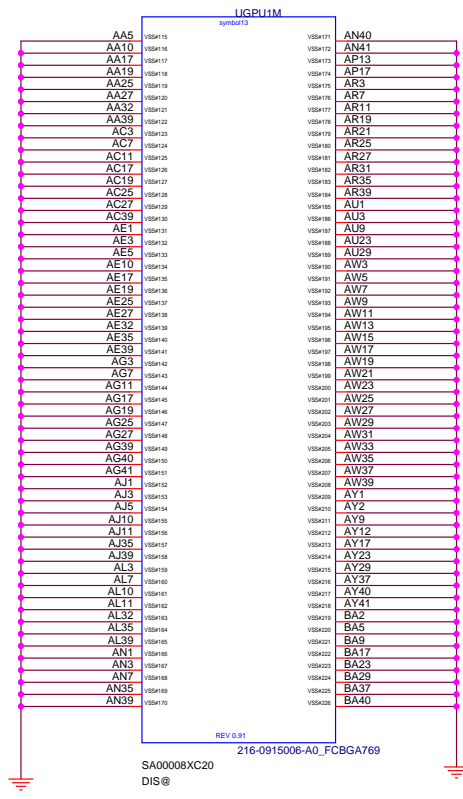


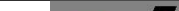
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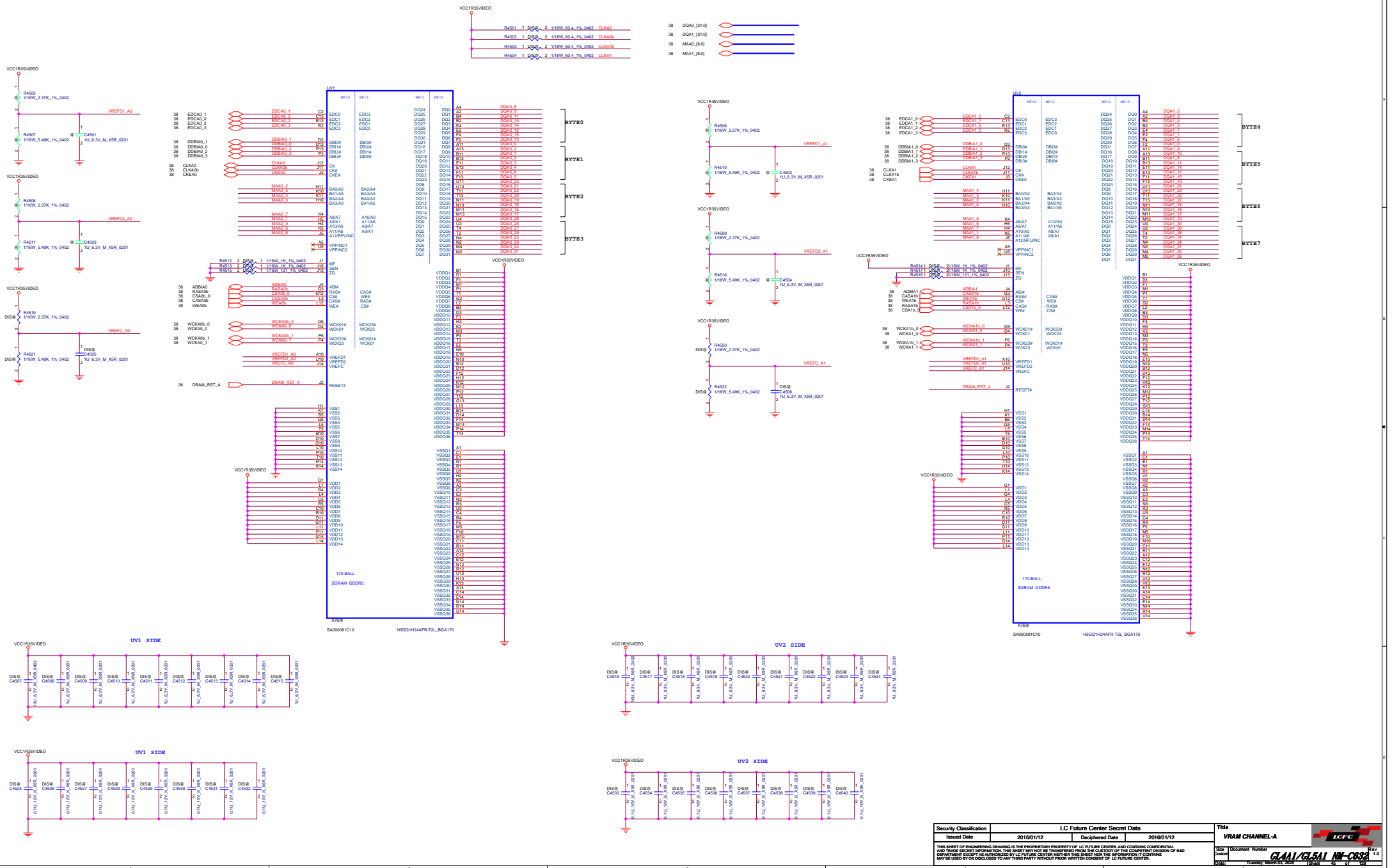
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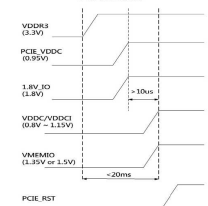
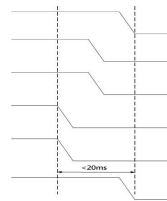
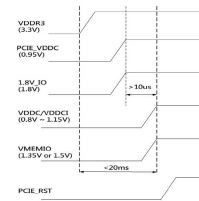
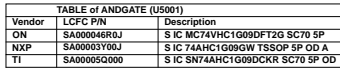
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					Date:	Tuesday, March 03, 2020	Sheet 49 of 128																																											
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Mos max 2.5A , But 0.95VS_VGA EDC is 3A
Nominal at 0.95 V, Need check
support up to 1.05 V functionally.

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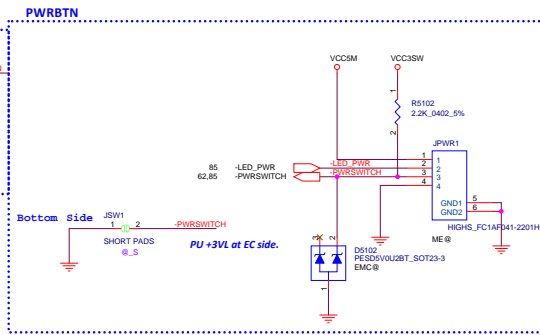
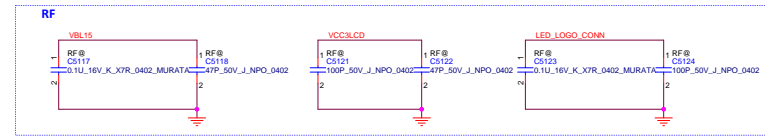
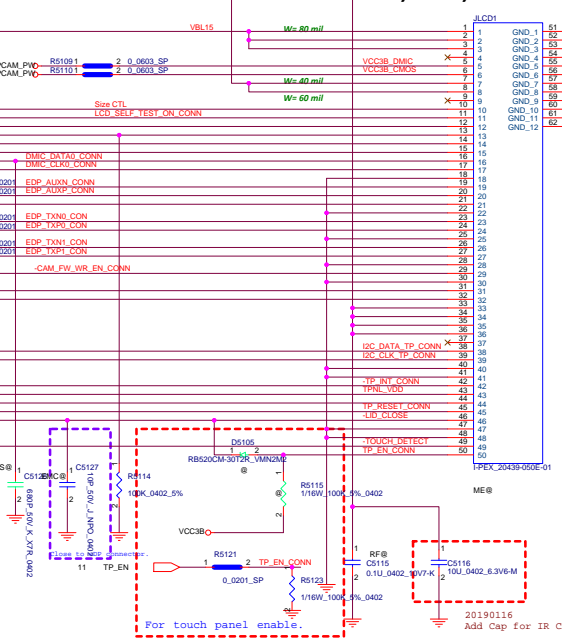
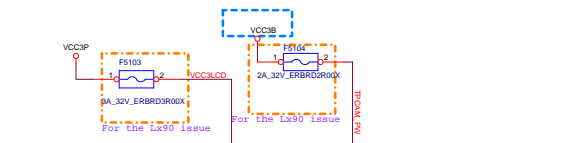
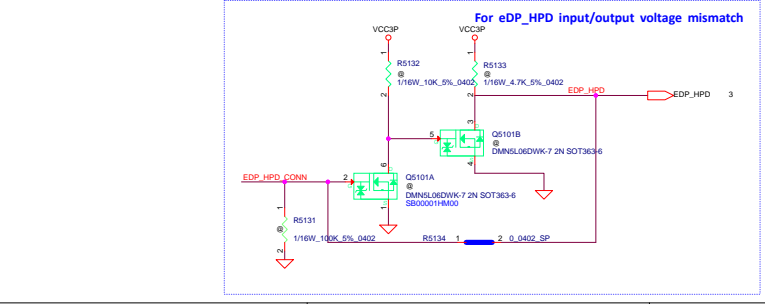
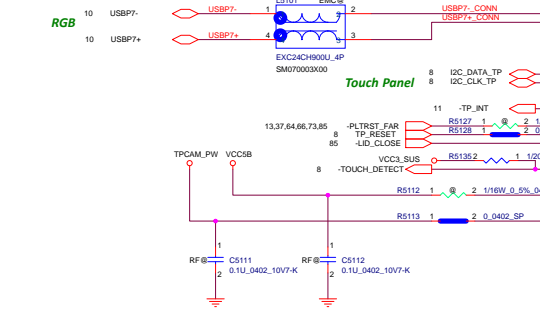
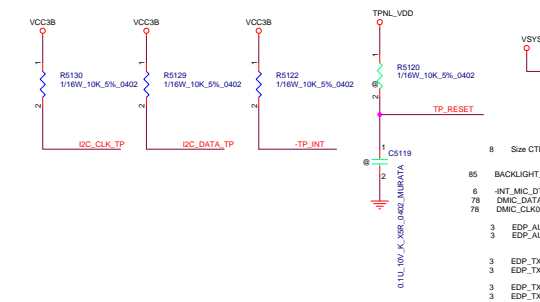
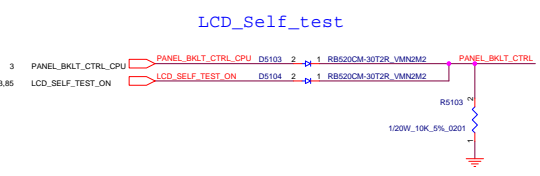



TABLE of POWER SWITCH (U5101)		
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GMT	SA000074R00	S IC G524B1T11U SOT23 5P POWER SWITCH
SILERGY	SA000074P00	S IC SYG288C20AAC SOT23 5P POWER SWITCH
RICHTEK	SA0000A2M00	S IC RT9742CGJ5 TSOT-23 5P PWR SW




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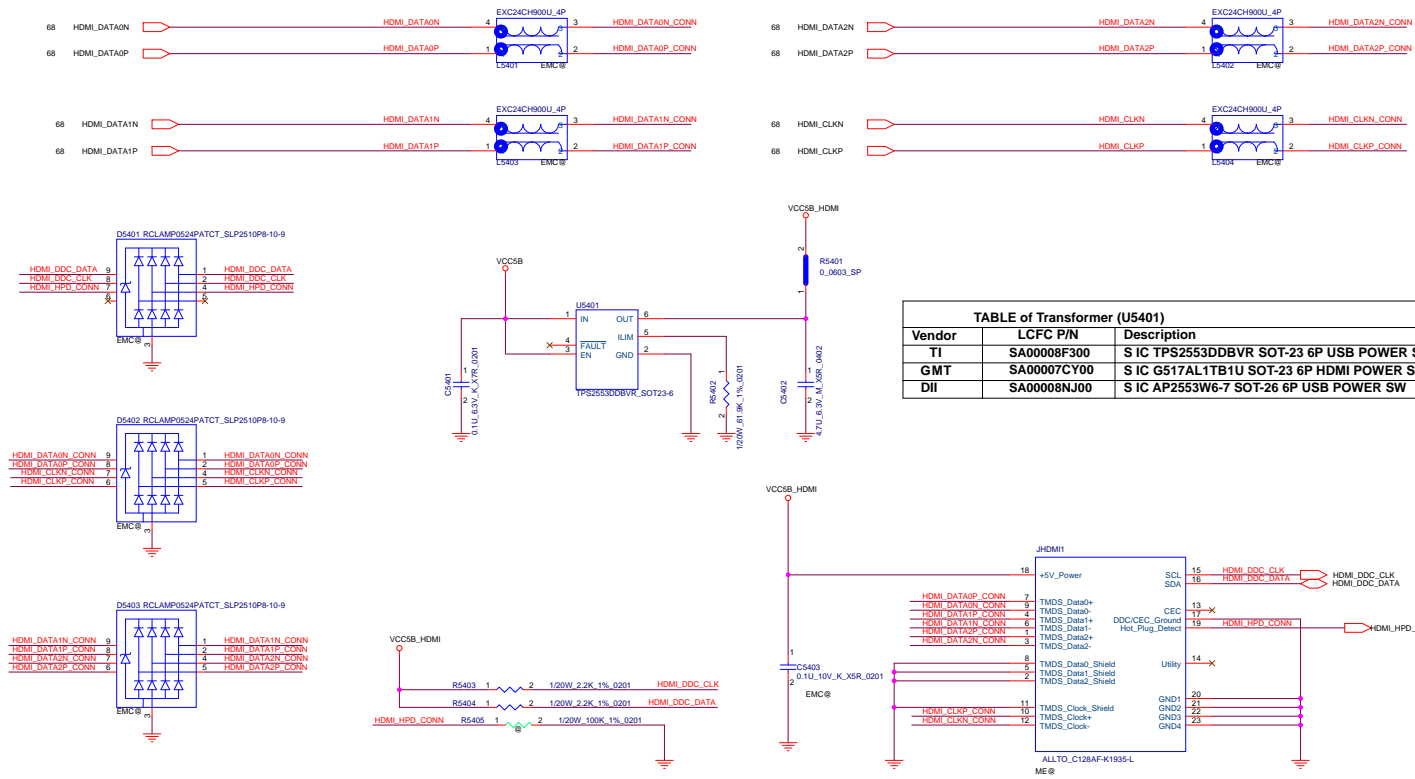


Figure 7-12. HDMI 1.4* HPD Active Level Shifter Design Recommendation

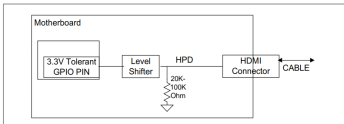
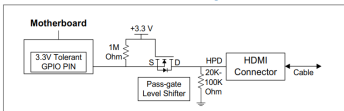



Figure 7-13. HDMI 1.4* HPD Cost Reduced Level Shifter Design Recommendation



Note: 3.3V transistor gate supply must turn off when CPU power is turned off.

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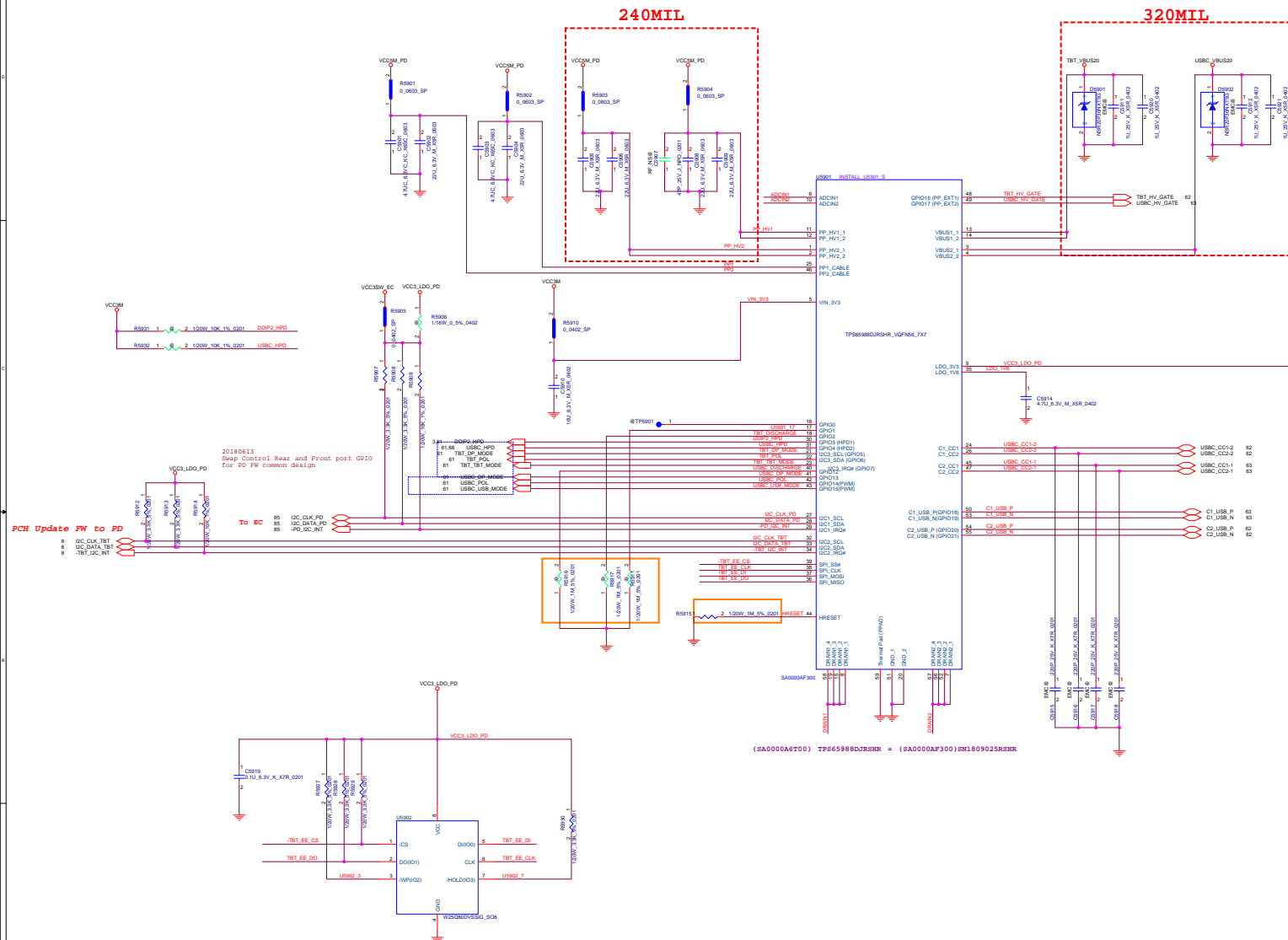


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ADCIN1 BUS POWER CONFIGURATION

DIV MIN	DIV MAX	CONFIGURATION
0.00	0.18	BP_NoResponse
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

← LOGIC

ADCIN2 I2C Address Setting

DIV MIN	DIV MAX	ADC_ADDR_DECODE_C1	ADC_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

← LOGIC


I2C Address

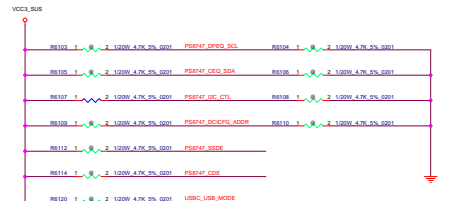
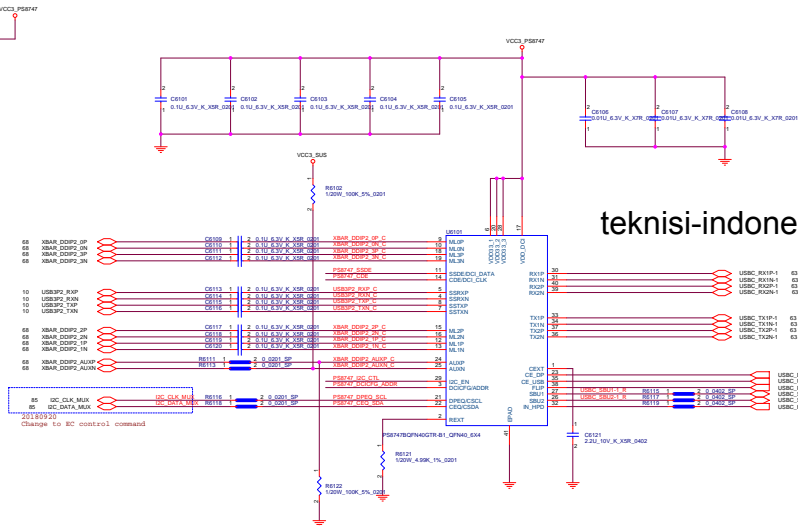
I2C1 (to EC)	TBT PORT	0X46/0X47
USBC_PORT	0X4E/0X4F	
I2C2 (to AR)	TBT PORT	0X70/0X71
USBC_PORT	0X7E/0X7F	

TABLE of PD ROM (U5902)

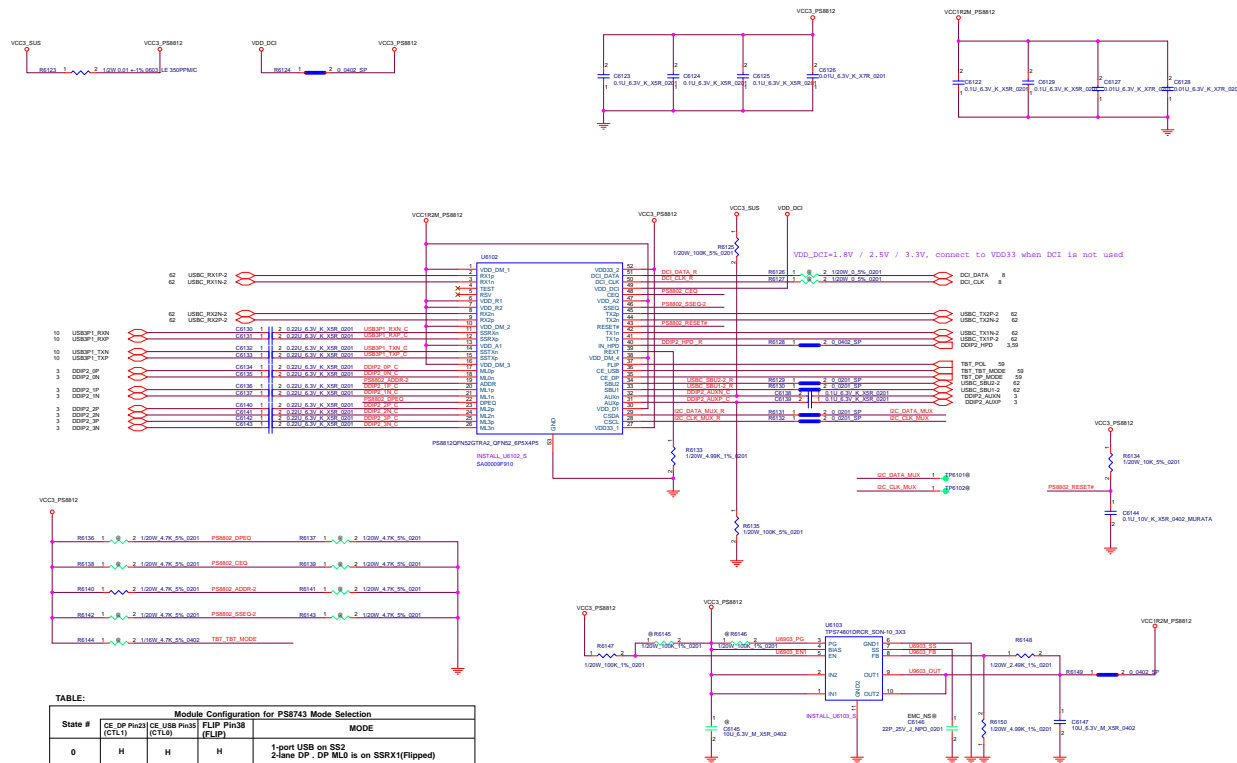
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Winbond	SA000078K00	S IC FL 8M W25Q80DVSSIG SOIC 8P SPI ROM
MXIC	SA000068B00	S IC FL 8M MX25L8006EM2I-12G SOP 200MIL
GIGADEVICE	SA000068A10	S IC FL 8M GD25Q80CSIGR SOP 8P 208MIL

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State #	Module Configuration for PS8743 Mode Selection				MODE
	CE_DP Pin32 (CT1)	CE_USB Pin33 (CT1)	FLIP Pin38 (FS1)		
0	H	H	H		1-port USB on SS2 2-lane DP, DP ML0 is on SSRX1(Flipped)
1	H	H	L		1-port USB on SS1 2-lane DP, DP ML0 is on SSRX2(Un-flipped)
2	H	L	H		4-lane DP, DP ML0 is on SSRX1(Flipped)
3	H	L	L		4-lane DP, DP ML0 is on SSRX2(Un-flipped)
4	L	H	H		1-port USB only on SS2 channels (Flipped)
5	L	H	L		1-port USB only on SS1 channels (Un-flipped)
6	L	L	H		Chip power down
7	L	L	L		Chip power down



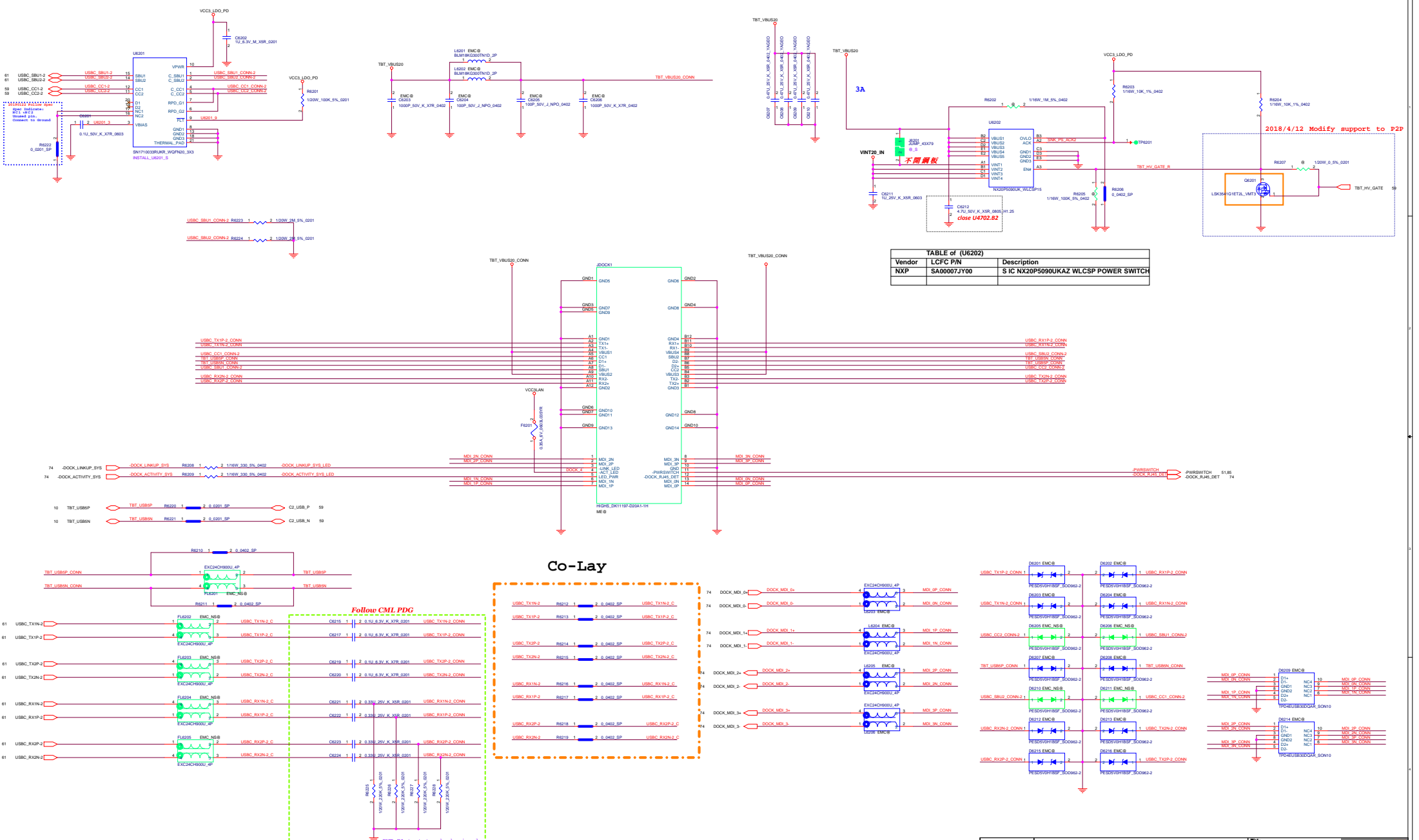


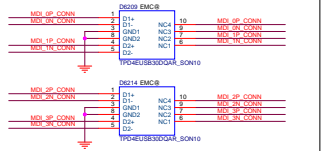
TABLE of (U6202)		
Vendor	LCFC P/N	Description
NXP	SA00007JY00	S IC NX20P5090UKAZ WLCSP POWER SWITCH

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Doc#		CLAU/CL541			

2018/4/12 Modify support to P2P

Co-Lay

Follow CML PDG



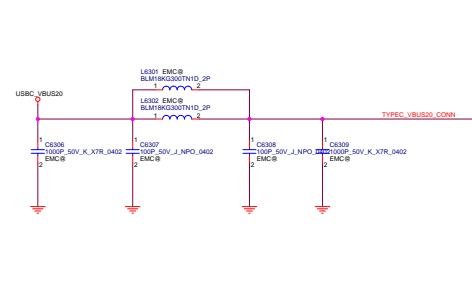
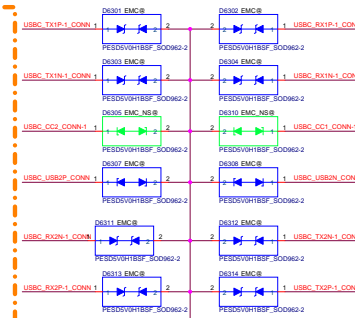
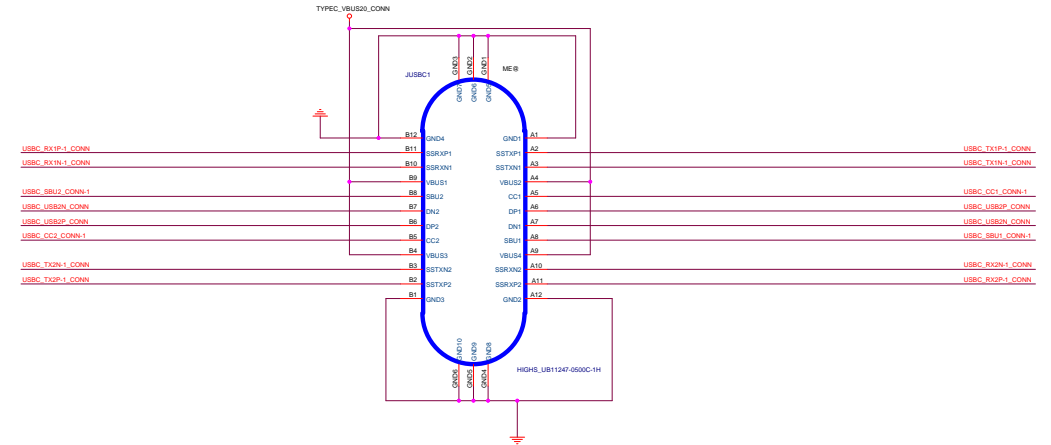
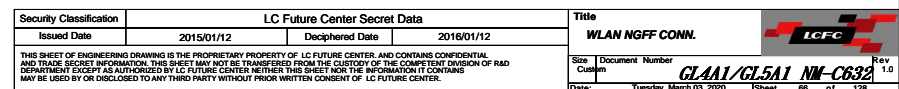


TABLE of PROTECTOR (U6301)		
Vendor	LCFC P/N	Description
TI	SA000093G00	S IC SN1710033RUKR WQFN PORT PROTECTOR



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				Sheet	67 of 128



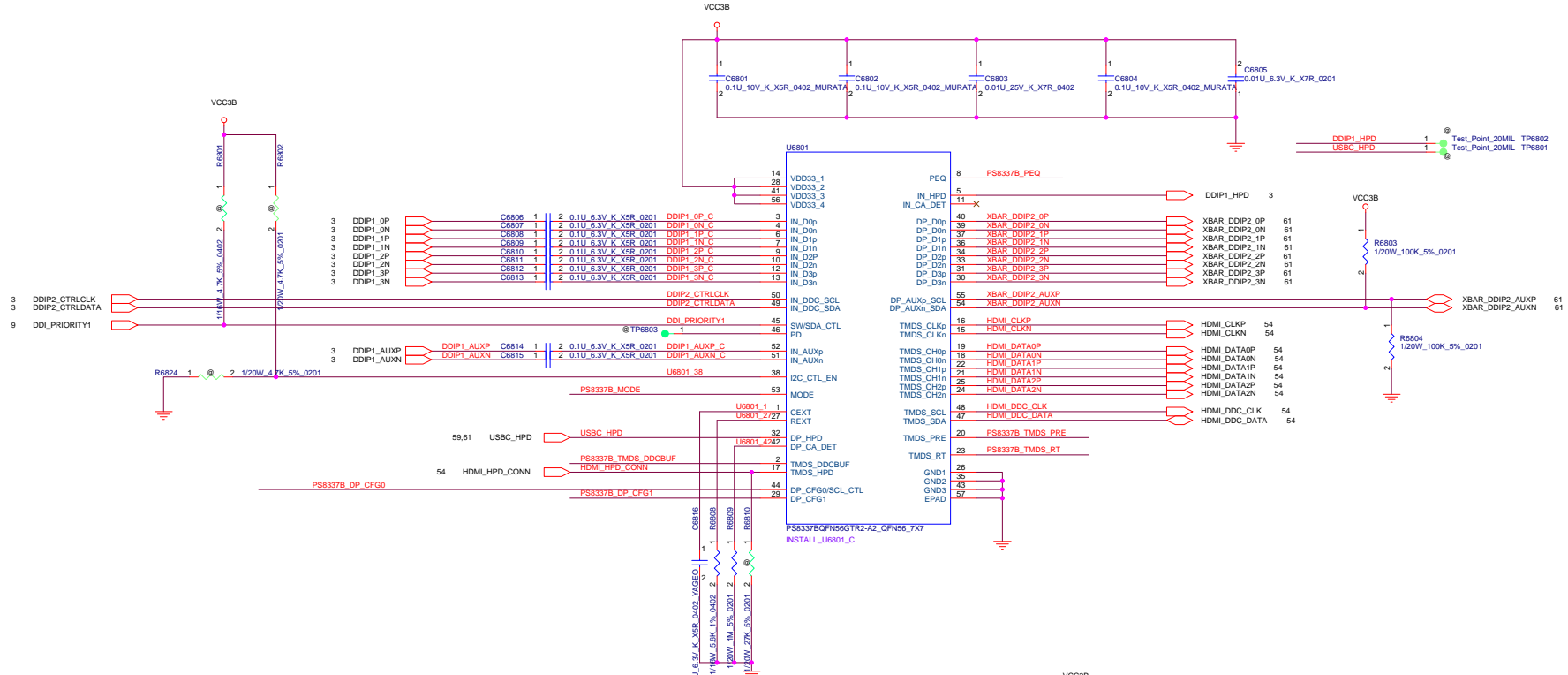
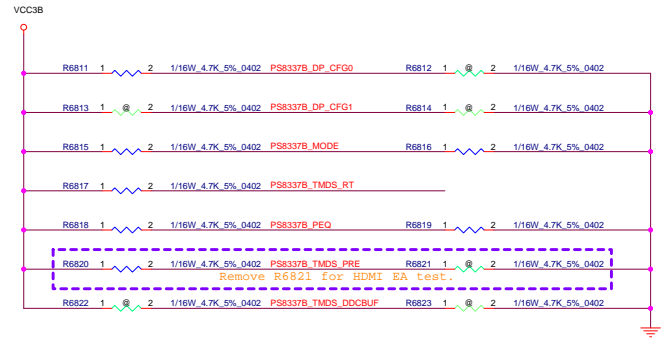


TABLE: Automatic Switching Mode (MODE=H/M)

SW(DDI_PRIORITY1)	
L	DP Port has higher priority when both ports are plugged
H	TMDS Port has higher priority when both ports are plugged
MODE =	
H	: Automatic Switching mode, HDMI ID Disabled
M	: Automatic Switching mode, HDMI ID Enabled
L	: Control Switching mode, HDMI ID Disabled

← DEFAULT

← DEFAULT



USB AOU

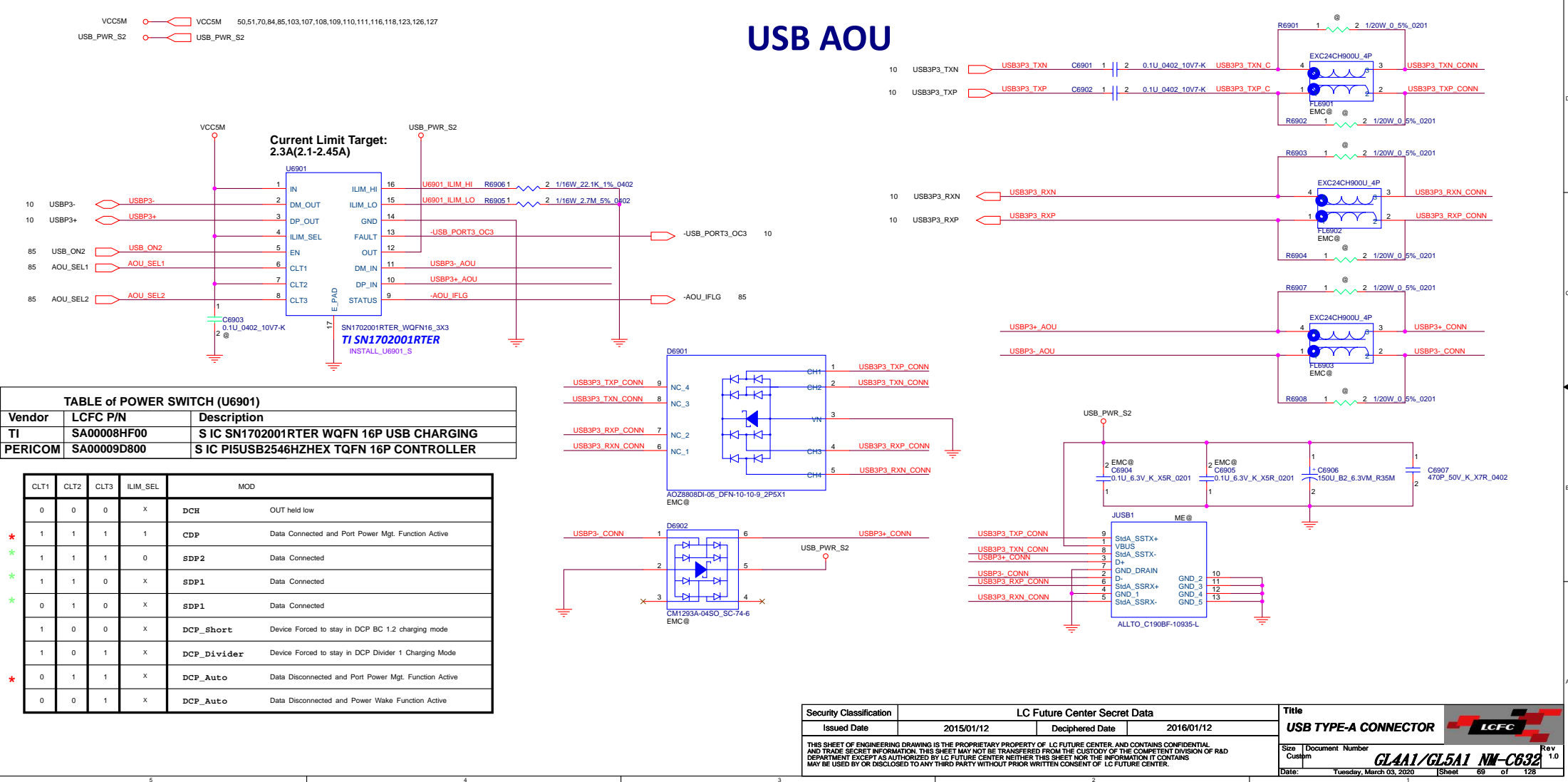
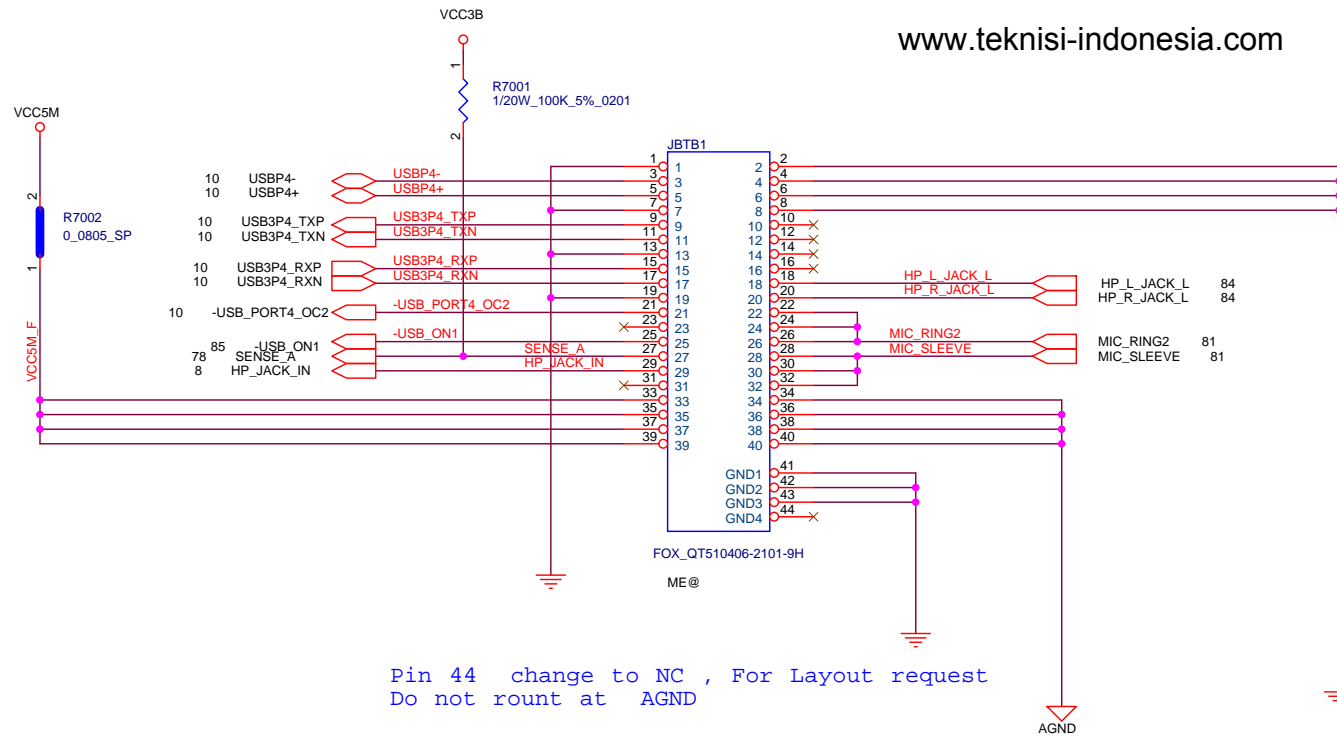



TABLE of POWER SWITCH (U6901)		
Vendor	LCFC P/N	Description
Ti	SA00008HF00	S IC SN1702001RTER WQFN 16P USB CHARGING
PERICOM	SA00009D800	S IC PI5USB2546HZHEX TQFN 16P CONTROLLER


CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active

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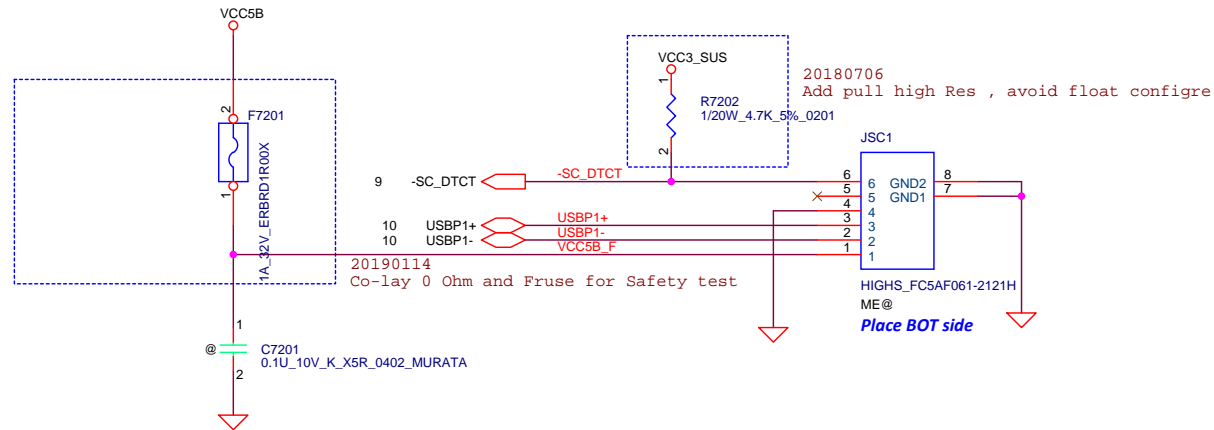


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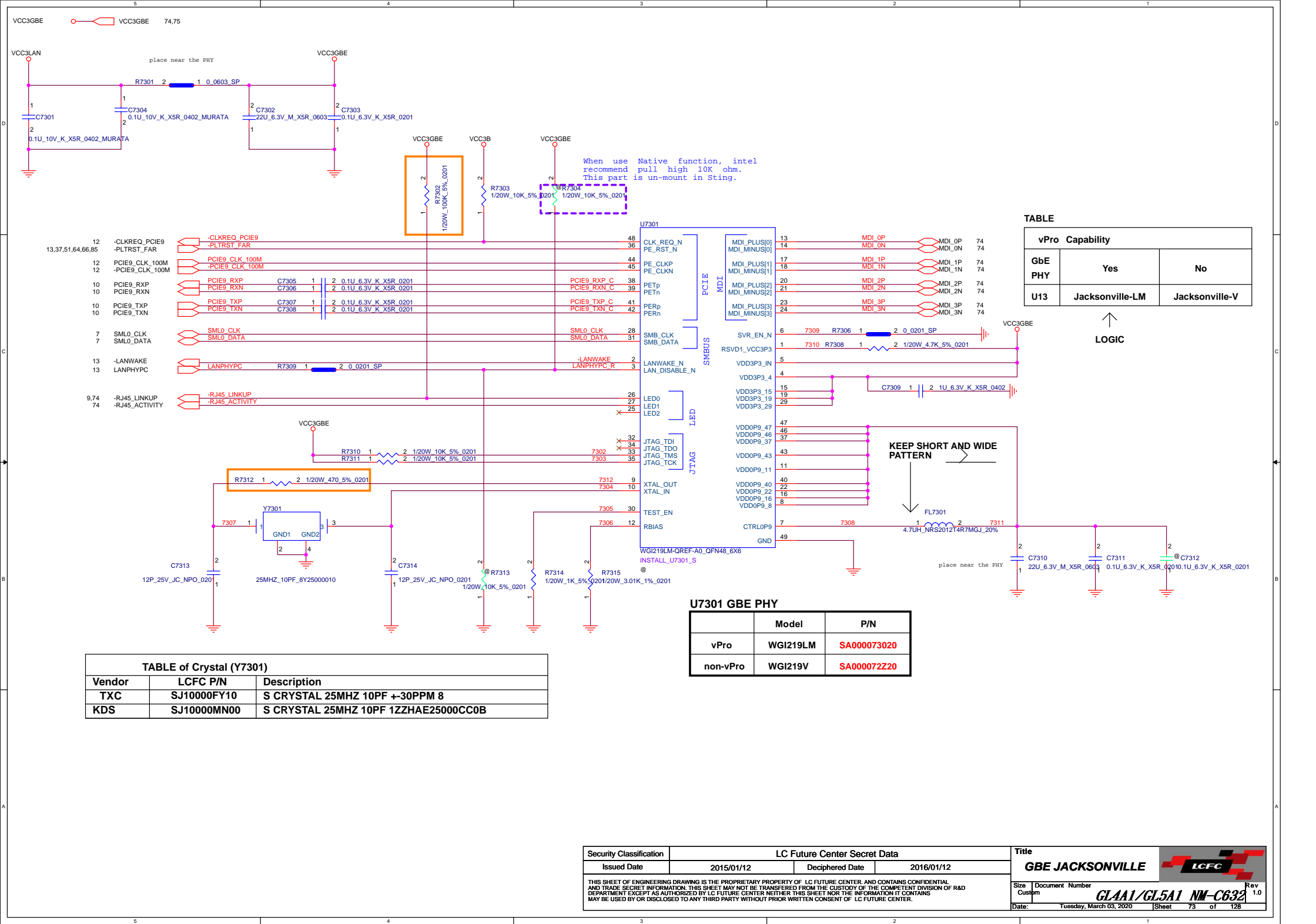
SMART CARD CONN.



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VCC3GBE VCC3GBE 73,75

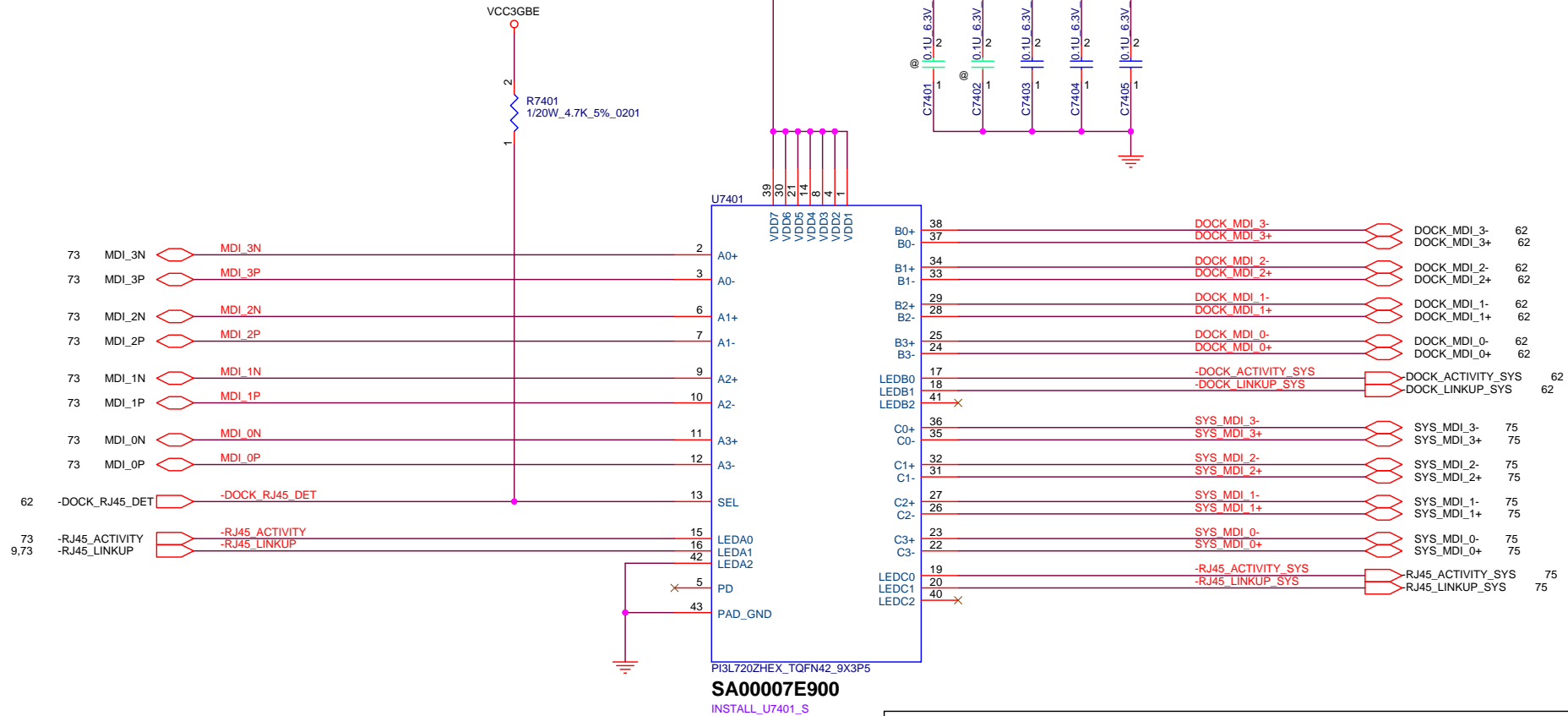


TABLE of LAN SWITCH (U7401)

Vendor	LCFC P/N	Description
PERICOM	SA00007E900	S IC PI3L720ZHE+CX TQFN GBE LA
TI	SA000072400	S IC TS3L501ERUAR WQFN 42P LAN


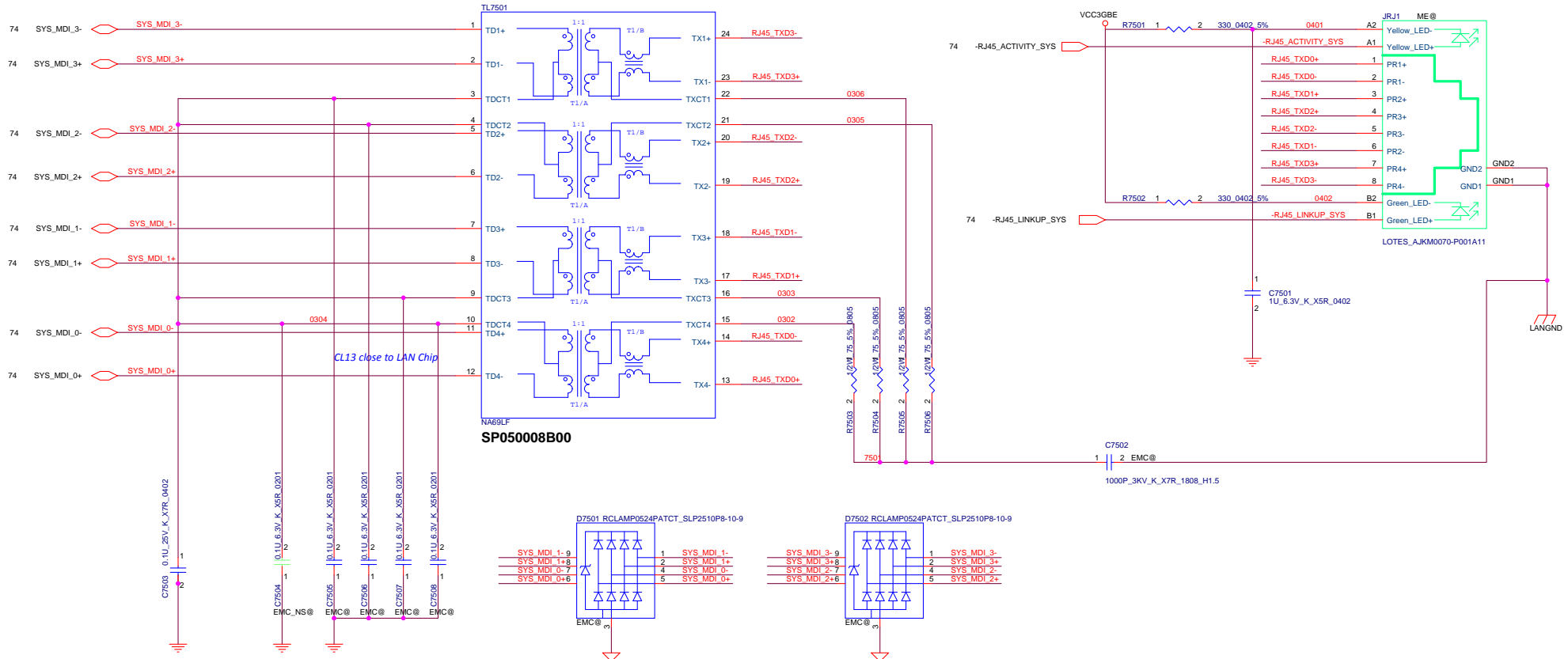
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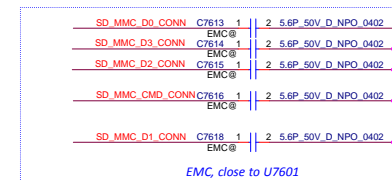
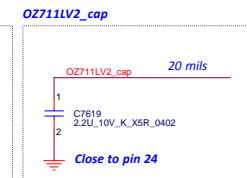
TABLE of Transformer (TL7501)		
Vendor	LCFC P/N	Description
BOTHHAND	SP050008B00	S X'FORM_ NA0069R LF LAN
TAIMAG	SP050009U00	S X'FORM_ IH-189-G LAN

LAN X' FORM

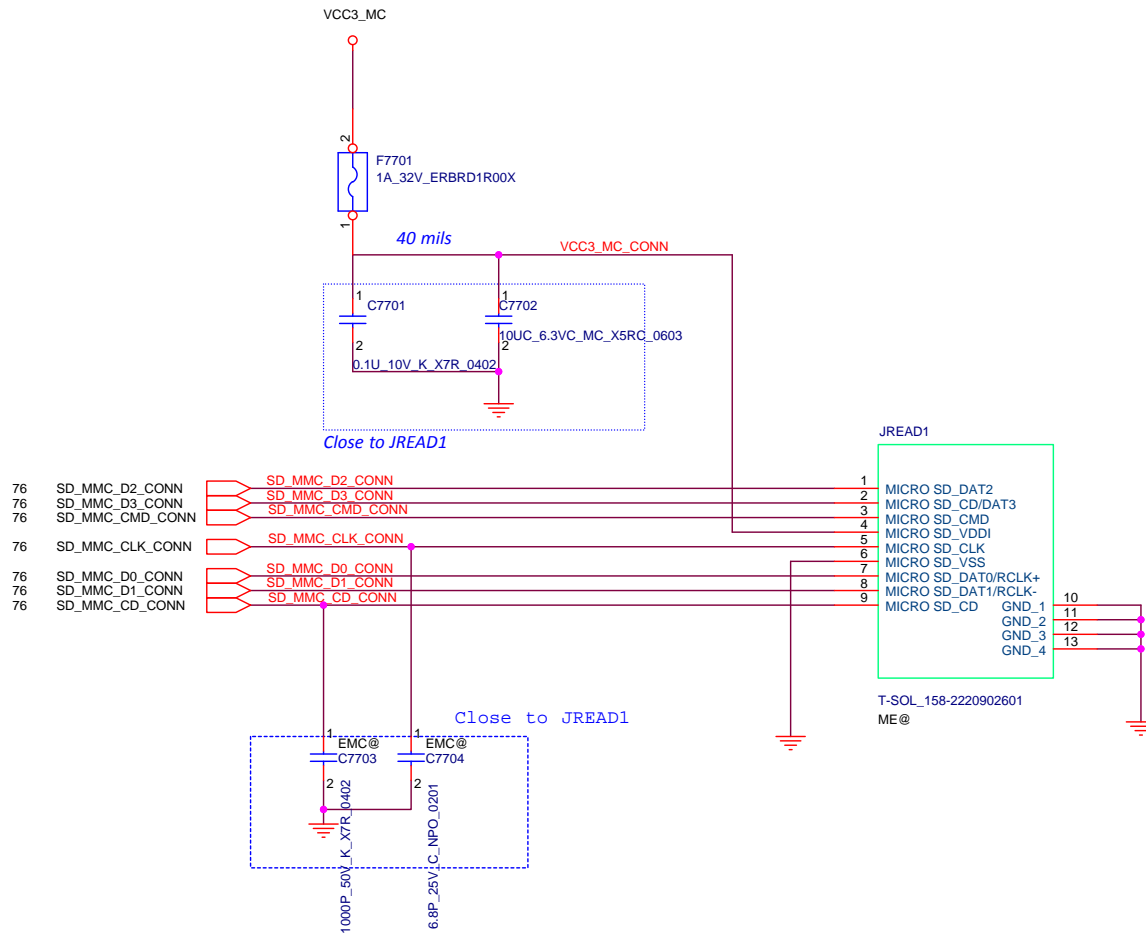
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VCC3_MC VCC3_MC 76

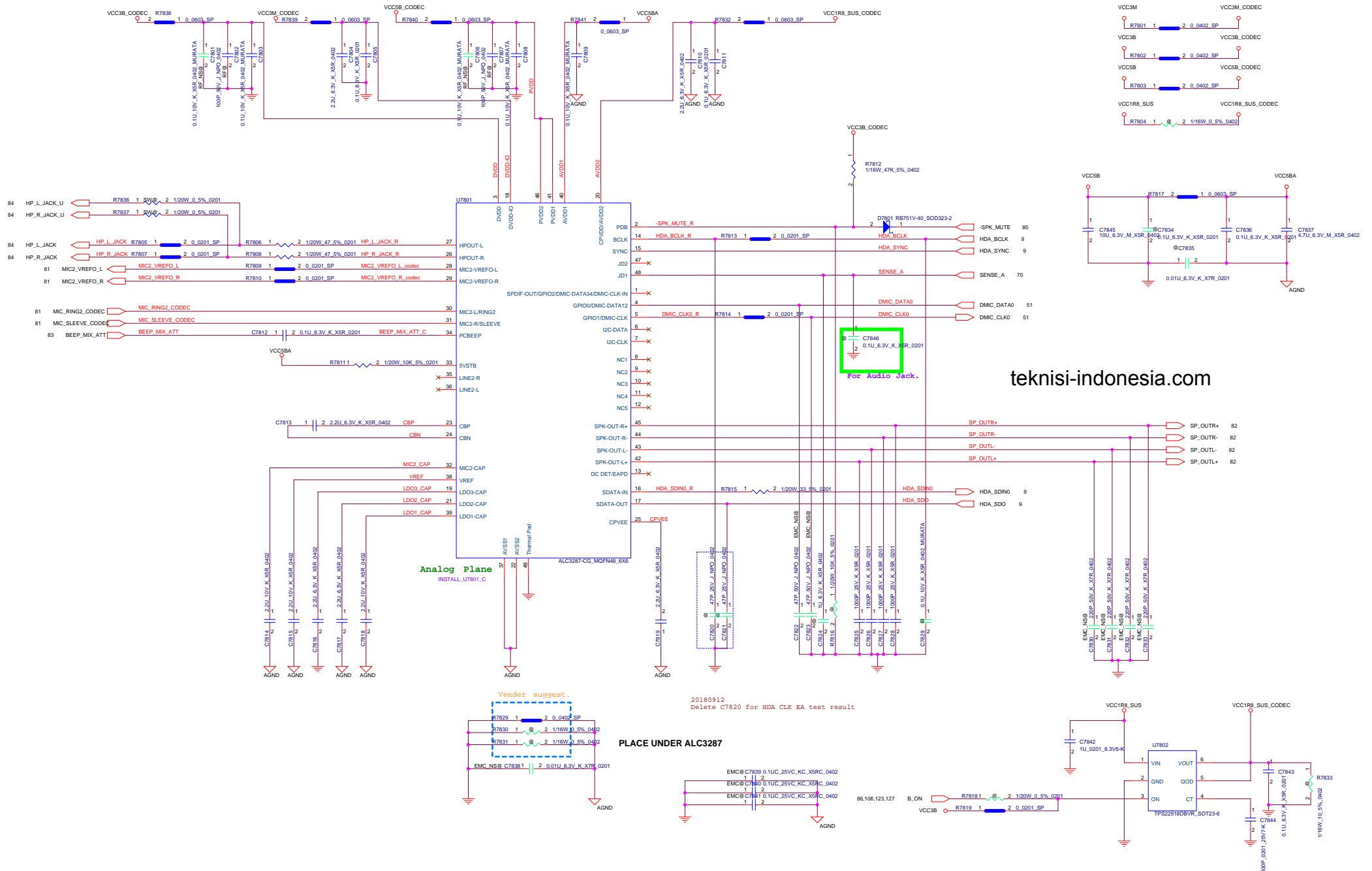


Mode	Detect
Normal	short
Card Insert	open


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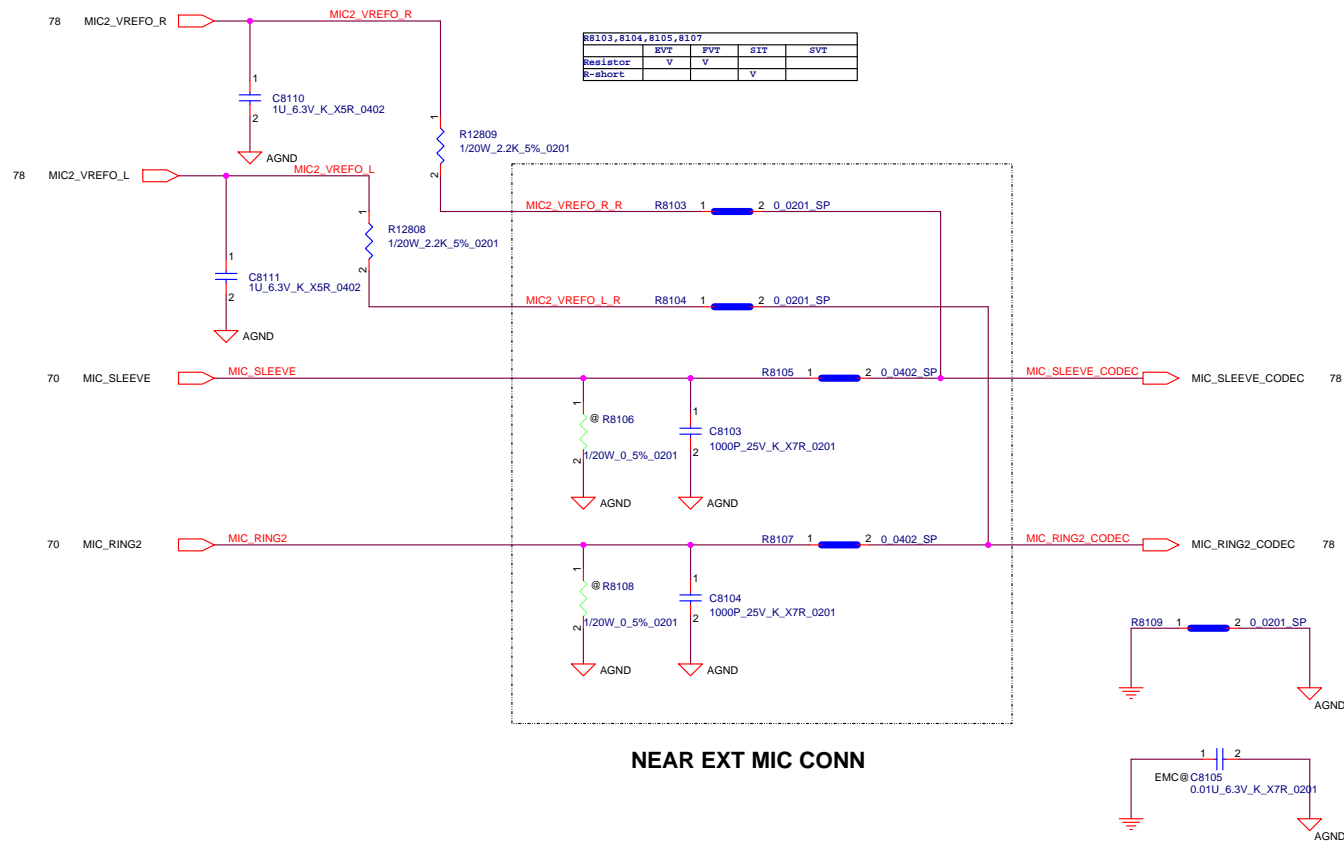


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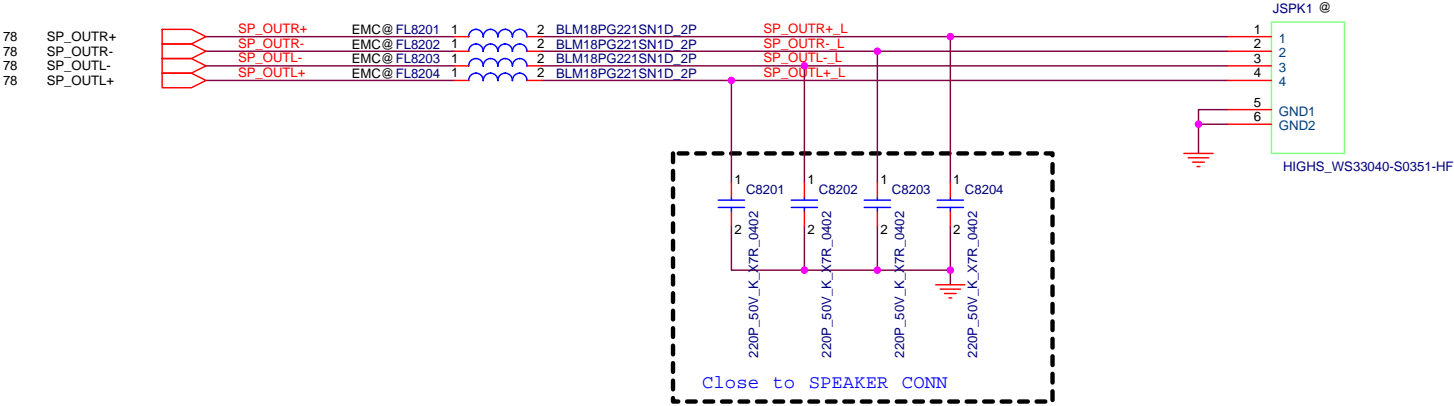
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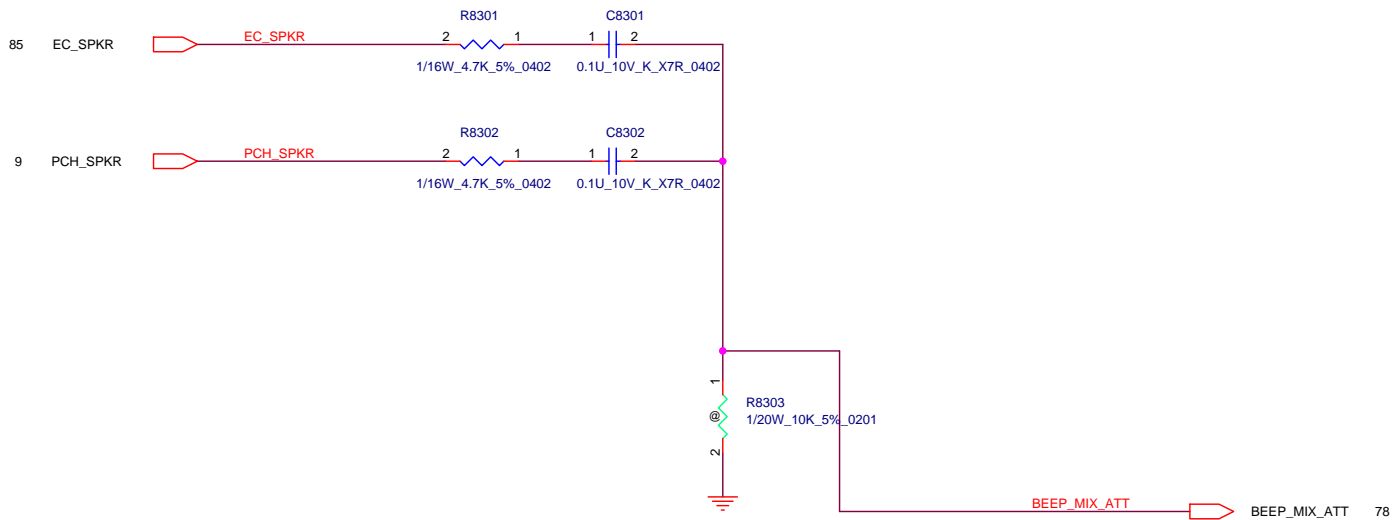



SPK CONN.



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Audio Beep



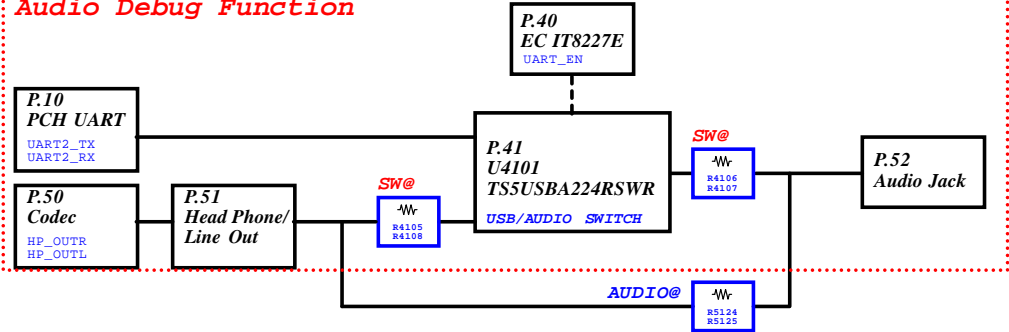
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				Date: Tuesday, March 03, 2020	Sheet 83 of 128

FUNCTION TABLE

A _{SEL}	V _{AUDIO}	V _{BUS}	L,R	D+, D-
L	L	L	OFF	OFF
L	L	H	OFF	OFF
L	H	L	ON	OFF
L	H	H	OFF ⁽¹⁾	ON
H	L	L	OFF	OFF
H	L	H	OFF	OFF
H	H	L	ON	OFF
H	H	H	ON	OFF

(1) 100Ω shunt resistors are enabled in this state.

Audio Debug Function



AUDIO DEBUG PORT

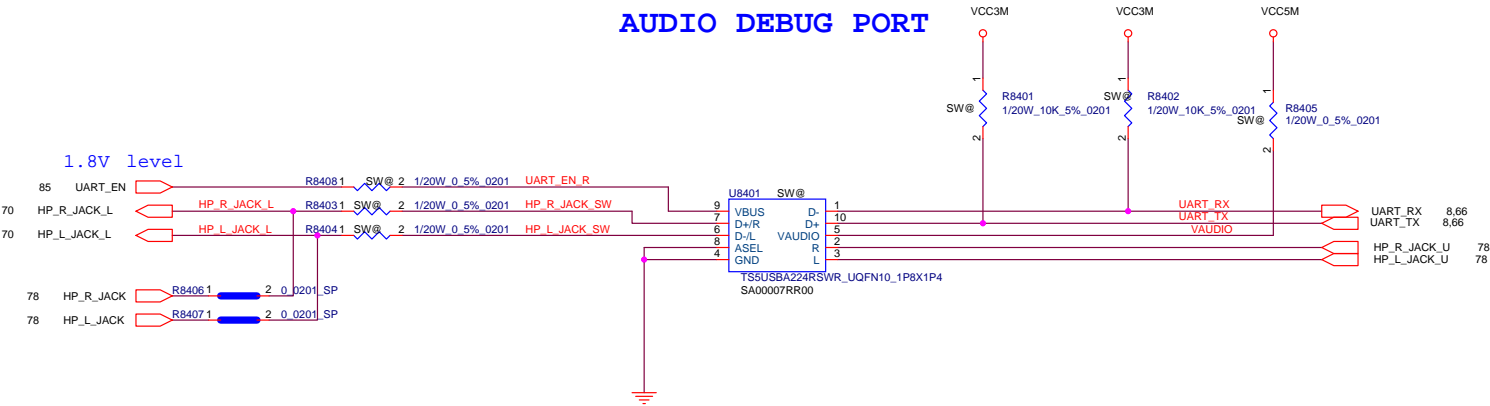
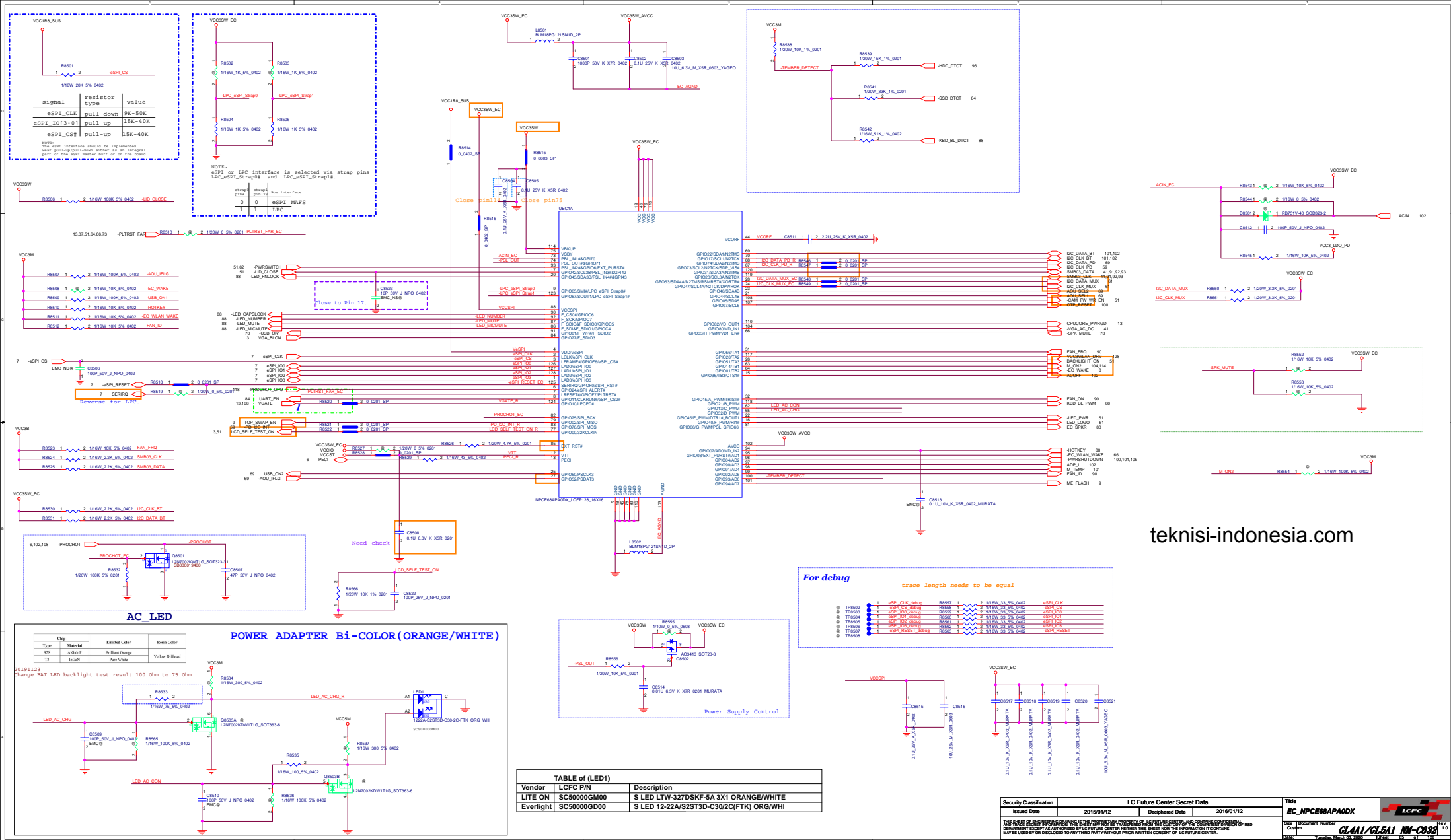


TABLE:

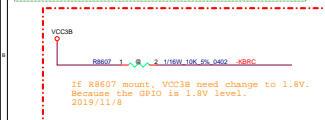
Mode	Audio	UART
UART_EN	L	H


TABLE:

Part Name	For NPI	For MP
U8401 SW@	ASM	NA
R8403 SW@	ASM	NA
R8404 SW@	ASM	NA
R8401 SW@	ASM	NA
R8402 SW@	ASM	NA
R8405 SW@	ASM	NA
R8506 AUDIO@	NA	ASM
R8507 AUDIO@	NA	ASM



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Doc No	NPCE689A00DX	Rev	1.0
Customer	GALAXY/GE541		NV-C836
Date	Tuesday, March 08, 2020	OS	61 72 12



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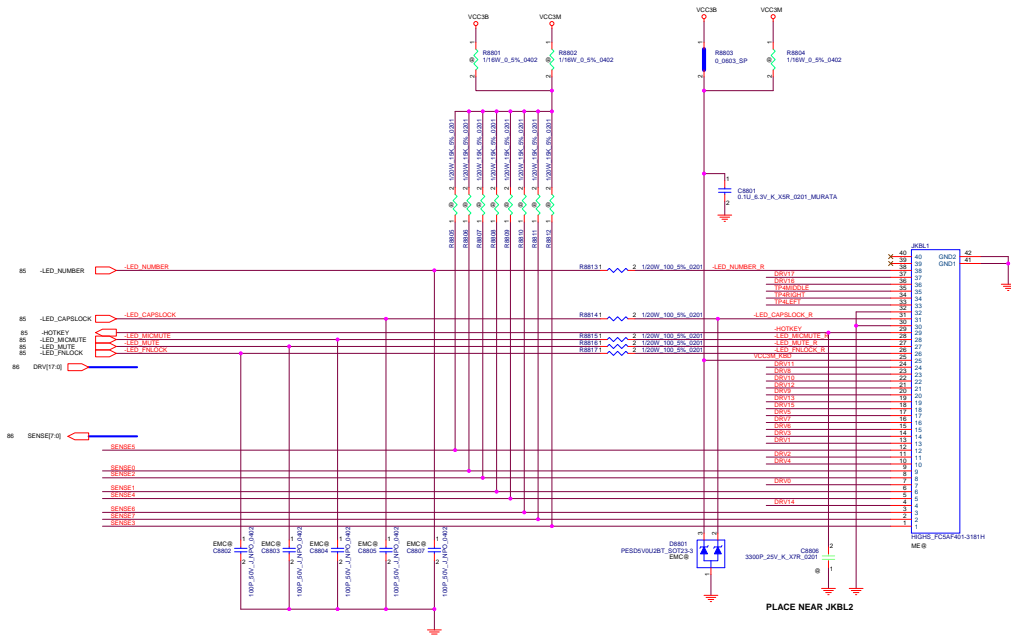
Size	Document Number	Rev
11x17	GC411/CL541 NW-C832	1.0

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				<div><div>Sheet</div><div>87</div><div>of</div><div>128</div></div>	



Keyboard CONN



Assign	Purpose
Vcc	Vcc 3V for LED
LED1	LED for FnLk
LED2	LED for F1
LED3	LED for F4
LED4	LED for CapsLk
LED5	LED for NumLock

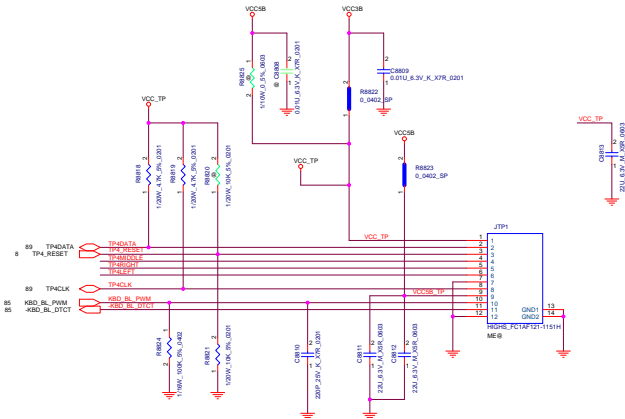
Assign	Purpose
MC	Common pin for TrackPoint click button
M1	Left button
M2	Right button
M3	Center button

Pin #	Assign
1	SENSE3
2	SENSE7
3	SENSE6
4	DRV14
5	SENSE4
6	SENSE1
7	DRV0
8	SENSE2
9	SENSE0
10	DRV4
11	DRV2
12	SENSE5
13	DRV1
14	DRV3
15	DRV6
16	DRV7
17	DRV5
18	DRV15
19	DRV13
20	DRV9
21	DRV12
22	DRV10
23	DRV8
24	DRV11
25	Vcc
26	LED1
27	LED2
28	LED3
29	HOTKEY
30	GND
31	LED4
32	MC
33	M1
34	M2
35	M3
36	DRV16
37	DRV17
38	LED5
39	NC
40	NC

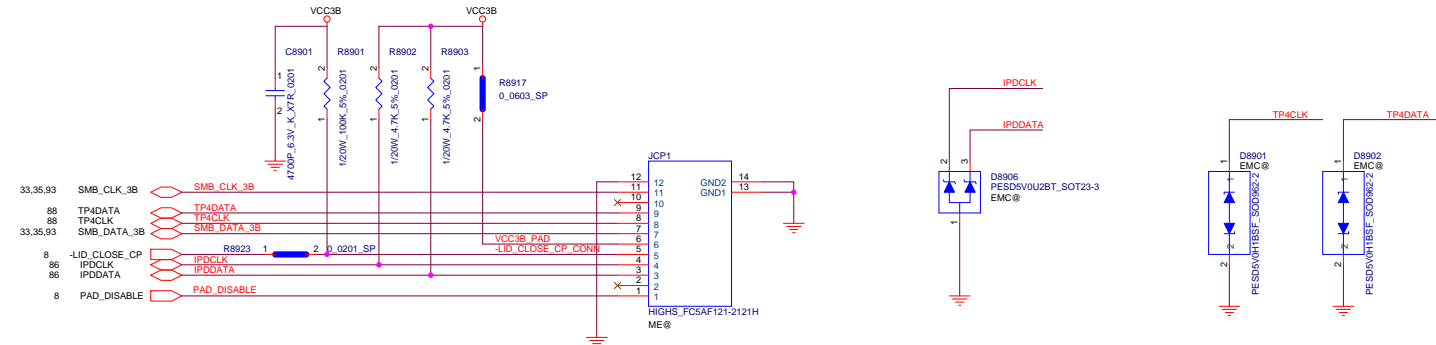
Track Point

TrackPoint and Backlight FPC Pin Assignment

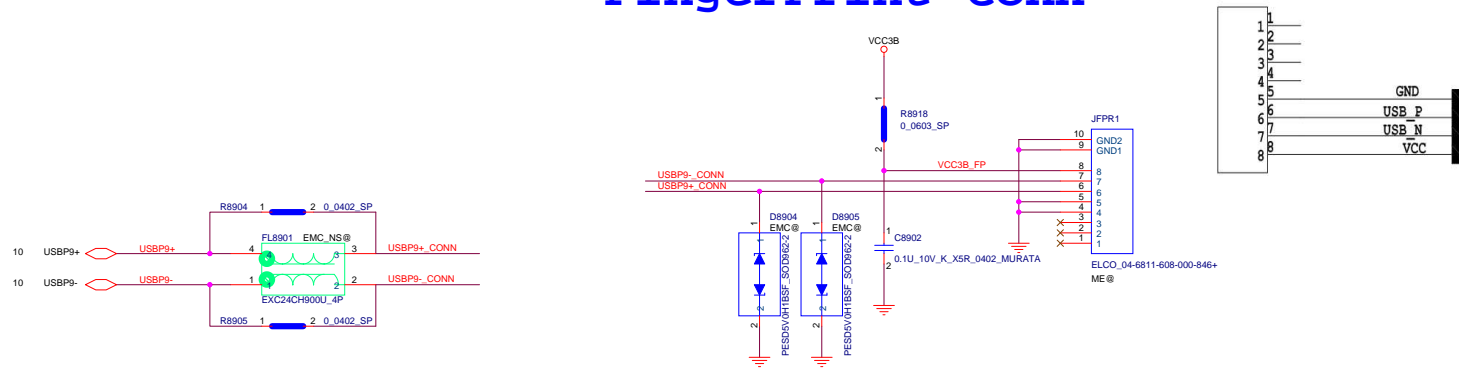
Pin #	Assign
1	VCC (3.3V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	LED VCC5 (5V)
10	LED PWM
11	Backlight detection
12	LED GND



Click Pad

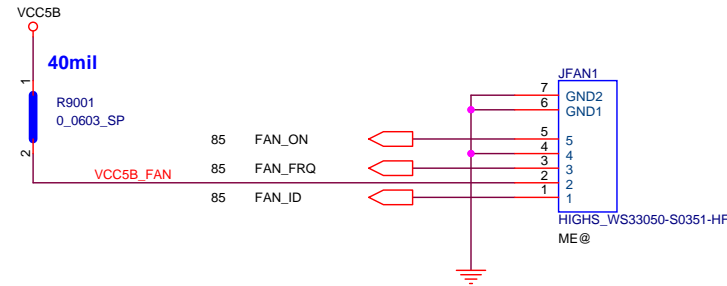


FingerPrint Conn

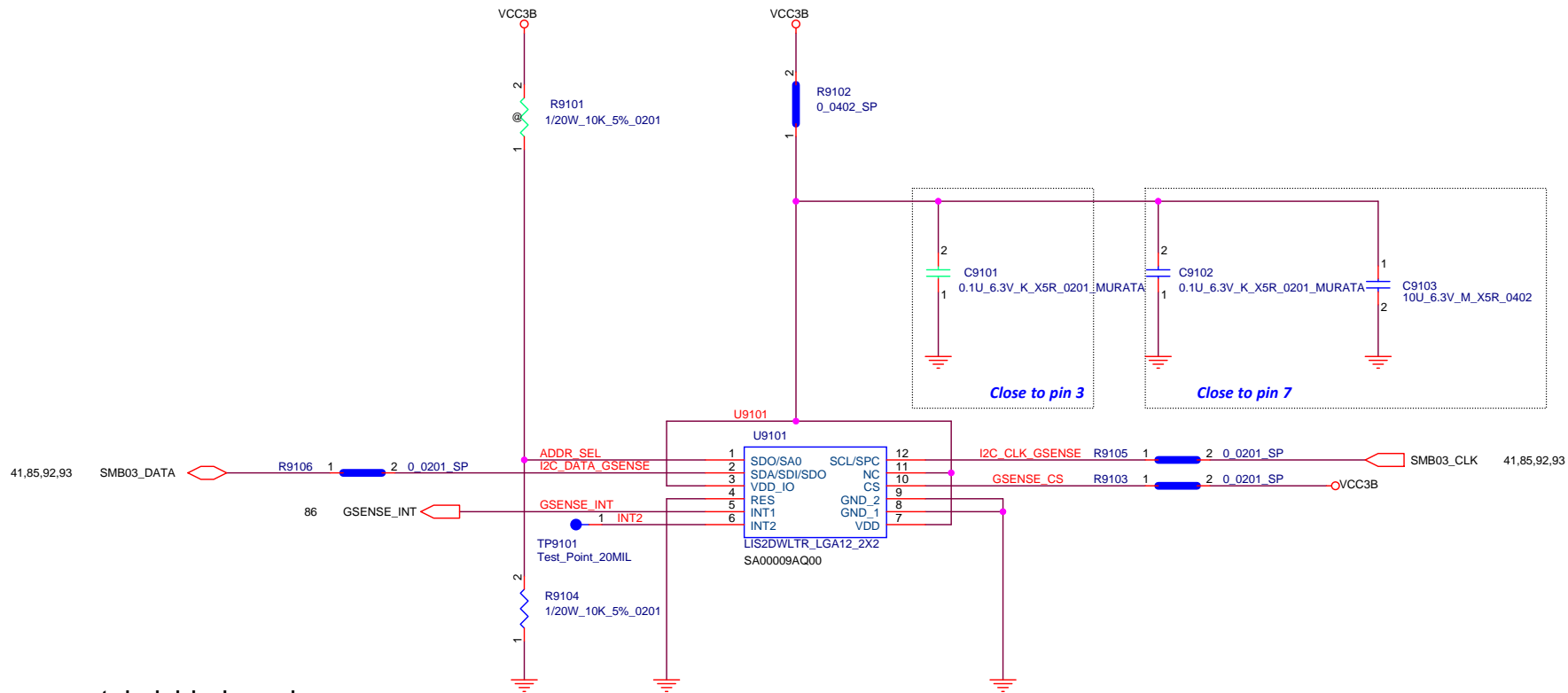


NFC

FAN CONN.



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				Date:	Rev
				Tuesday, March 03, 2020	1.0
				Sheet	90 of 128



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TABLE

TABLE of G-Sensor (U9101)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
BOSCH	BMA280	SA0000A1600

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
BMA280	H	0011001b(0x19)
	L	0011000b(0x18)

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Title		Rev	
APS G-SENSOR		1.0	
Size B	Document Number	GL4A1/GL5A1 NM-C632	
Date:	Tuesday, March 03, 2020	Sheet	91 of 128

Thermal Sensor Close to DIMM

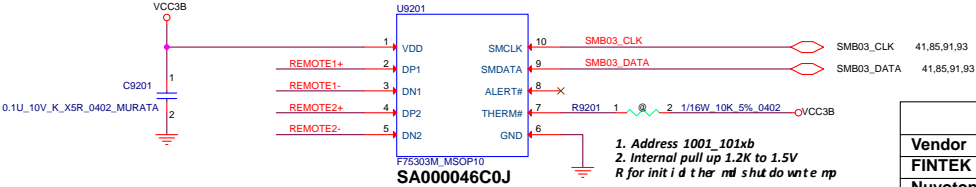
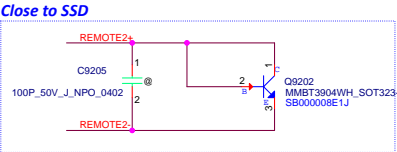
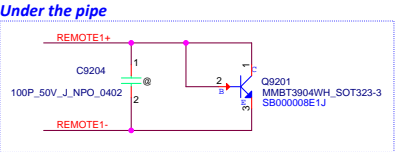
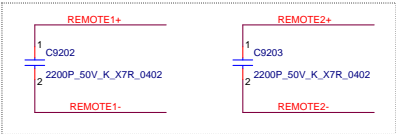


TABLE of Thermal Sensor (U9201)		
Vendor	LCFC P/N	Description
FINTEK	SA000046C0J	S IC F75303M MSOP 10P SENSOR
Nuvoton	SA000065D00	S IC NCT7719W MSOP 10P THERMAL SENSOR



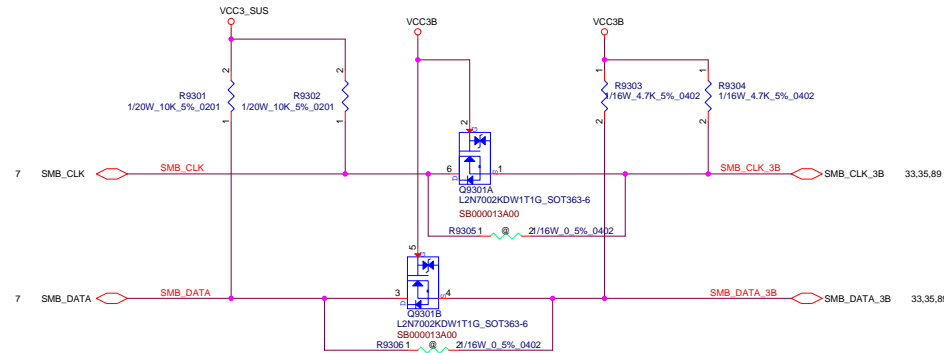
Trace width/space:10/10 mil
Trace length:<8"

TABLE of Thermal Sensor (Q9201,Q9202)		
Vendor	LCFC P/N	Description
PANJIT	SB000008E1J	S TR MMBT3904WH NPN SOT323-3
NXP	SB00000YV00	S TR PMST3904 NPN SOT323-3
LRC	SB00000ZJ00	S TR LMBT3904WT1G NPN SOT323-3

Security Classification	LC Future Center Secret Data		Title	
Issued Date	2015/01/12	Deciphered Date	2016/01/12	THERMAL SENSOR
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SMBus

DIMM1,DIMM2,CP



GPU, Thermal Sensor, Embedded Controller, G sensor

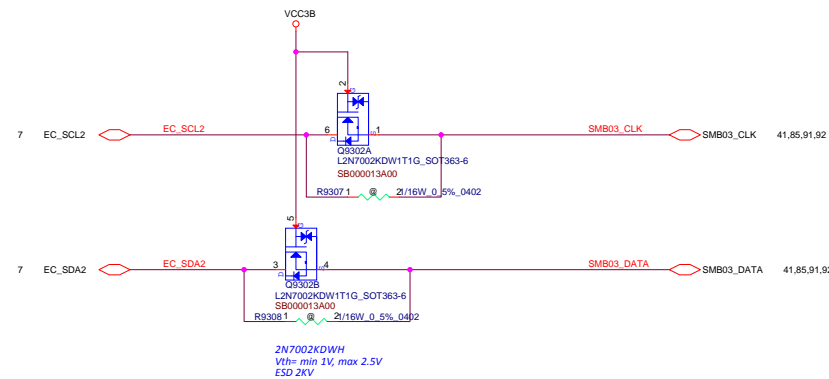



TABLE of U9301/U9302/U9303/U9304		
Vendor	P/N	LCFC P/N
TI	SN74LVC1G66DCK	SA00005BE0J
NXP	74LVC1G66GW	SA00007KS00
ONsemi	MC74VHC1G66DFT2G	SA00008JQ00


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Title		SMBUS SWITCH	
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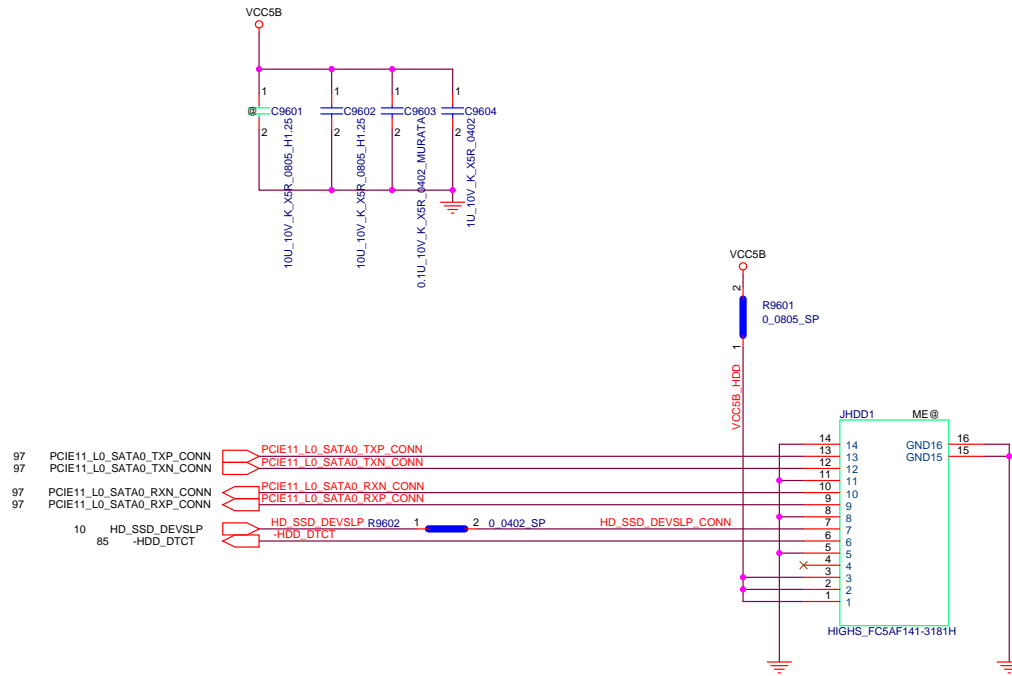
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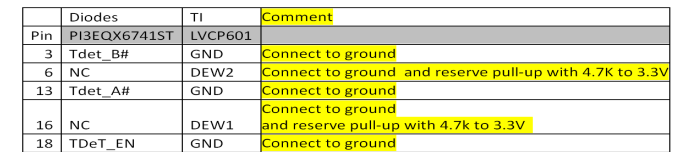
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SATA HDD CONN.



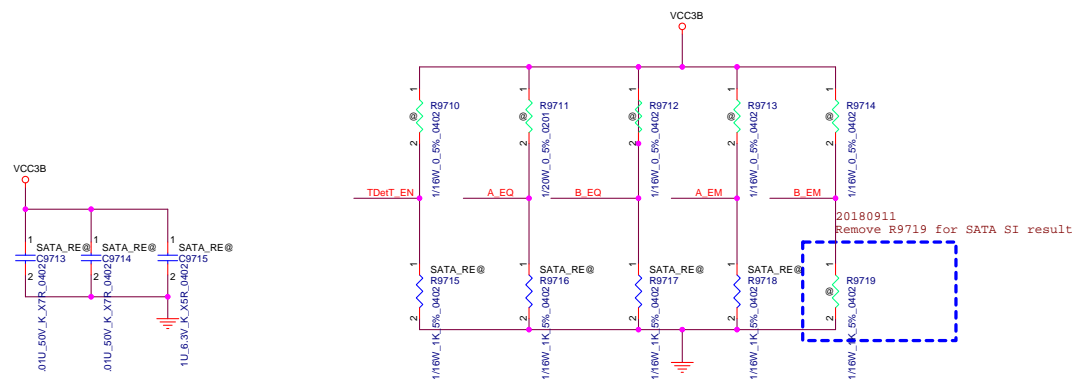
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	SATA HDD CONN	
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				Sheet 96 of 128	



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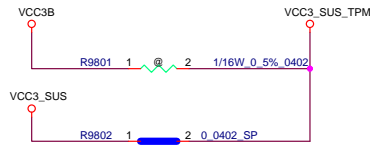
A_EQ/B_EQ	1.5 Gb/s	3 Gb/s	6Gb/s
0	1 dB	2.5 dB	3 dB
floating	2.5 dB	5 dB	6 dB
1	4 dB	7.5 dB	9 dB

A_EM/B_EM	3 Gb/s	6 Gb/s
0	500mV pp	600mV pp
1	500mV pp + 3dB Pre-emphasis	600mV pp + 1.5dB Pre-emphasis

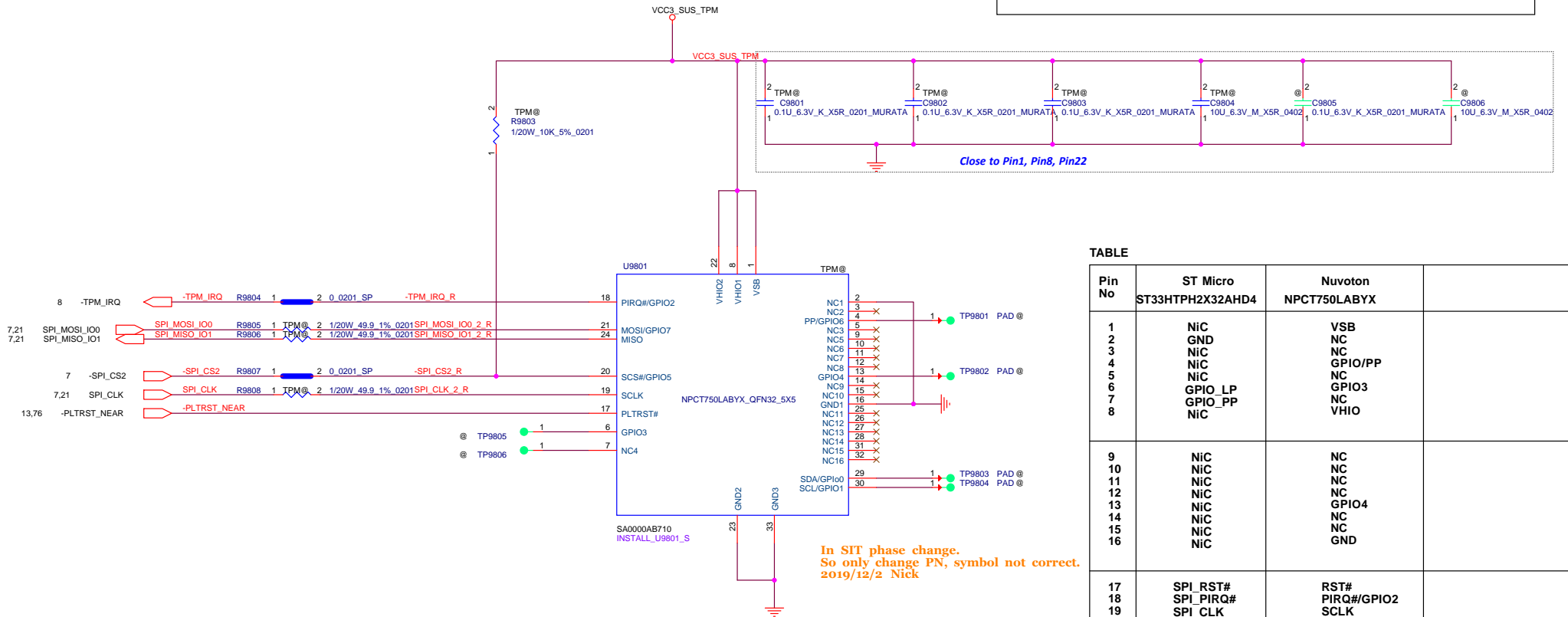
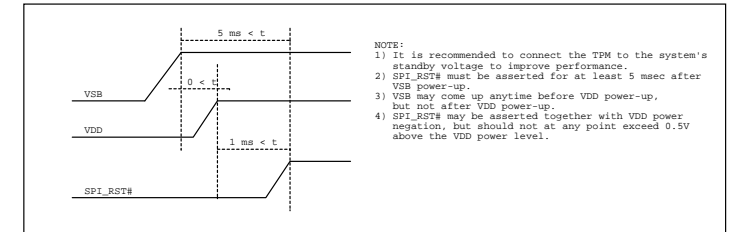


EL480/580 Setting					
TX EQ	TX EM			RX EQ	RX EM
3dB	0dB			3dB	0dB





NOTE:
Check timing sequence in SDV phase.



TABLE

Pin No	ST Micro ST33HTPH2X32AHD4	Nuvoton NPCT750LABYX	
1	NIC	VSB	
2	GND	NC	
3	NIC	NC	
4	NIC	GPIO/PP	
5	NIC	NC	
6	GPIO_LP	GPIO3	
7	GPIO_PP	NC	
8	NIC	VHIO	
9	NIC	NC	
10	NIC	NC	
11	NIC	NC	
12	NIC	GPIO4	
13	NIC	NC	
14	NIC	NC	
15	NIC	NC	
16	NIC	GND	
17	SPI_RST#	RST#	
18	SPI_PIRQ#	PIRQ#/GPIO2	
19	SPI_CLK	SCLK	
20	SPI_CS#	SCS#/GPIO5	
21	MOSI	MOSI/GPIO7	
22	VPS	VHIO	
23	GND	GND	
24	MISO	MISO	
25	NIC	NC	
26	NIC	NC	
27	NIC	NC	
28	NIC	NC	
29	NIC	SDA/GPIO1	
30	NIC	SDA/GPIO0	
31	NIC	NC	
32	NIC	NC	

TABLE of TPM (U9801)


Vendor	LCFC P/N	Description
ST	SA0000AB710	S IC ST33HTPH2X32AHD4 VQFN 32P TPM 2.0
NUVOTON	SA00008KS20	S IC NPCT750LABYX QFN 32P TPM 2.0




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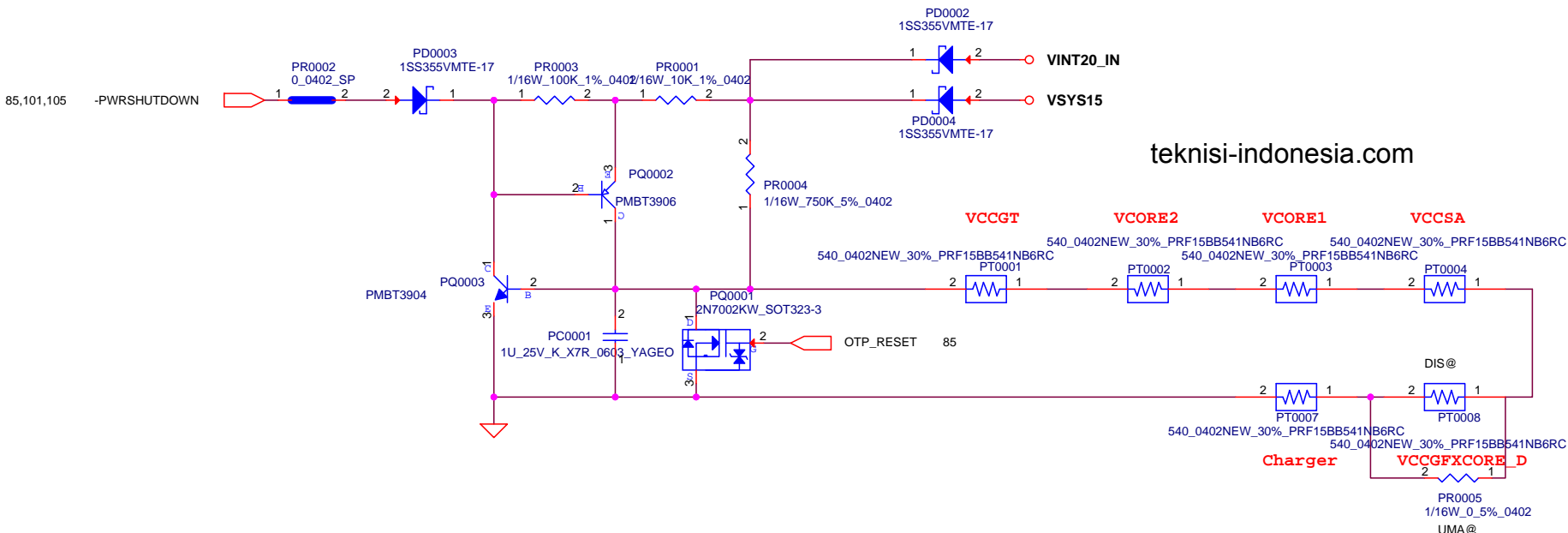
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For ME GND hole Screw Hole




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Custom		GL4A1/GL5A1		NW-C632		1.0
Date:		Tuesday, March 03, 2020		Sheet		99 of 128

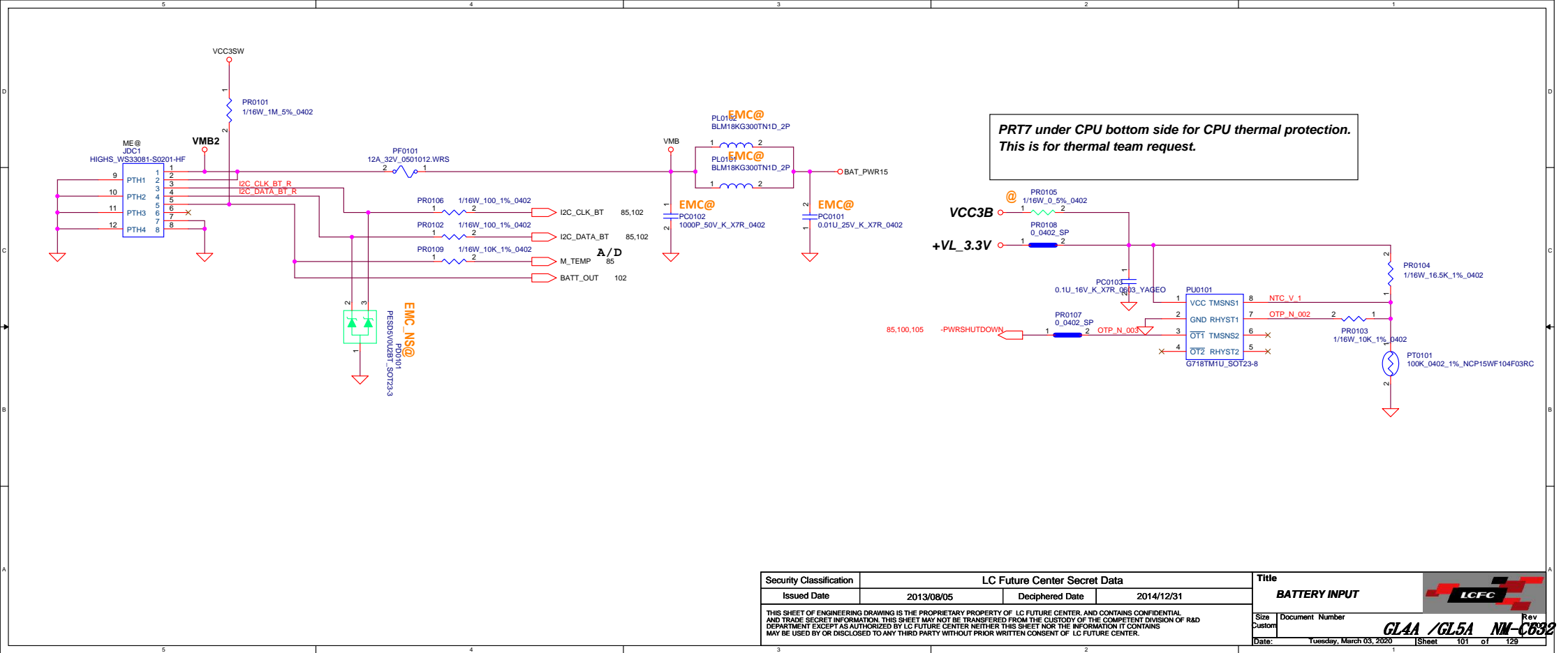
VINT20_IN		VINT20_IN	62,63,102
VSYS15		VSYS15	51,102,103,104,105,106,108,109,110,111,114,118,120
VCC3SW		VCC3SW	20,51,85,101,102,105,126,127
RTCVCC		RTCVCC	13,16,20

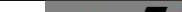


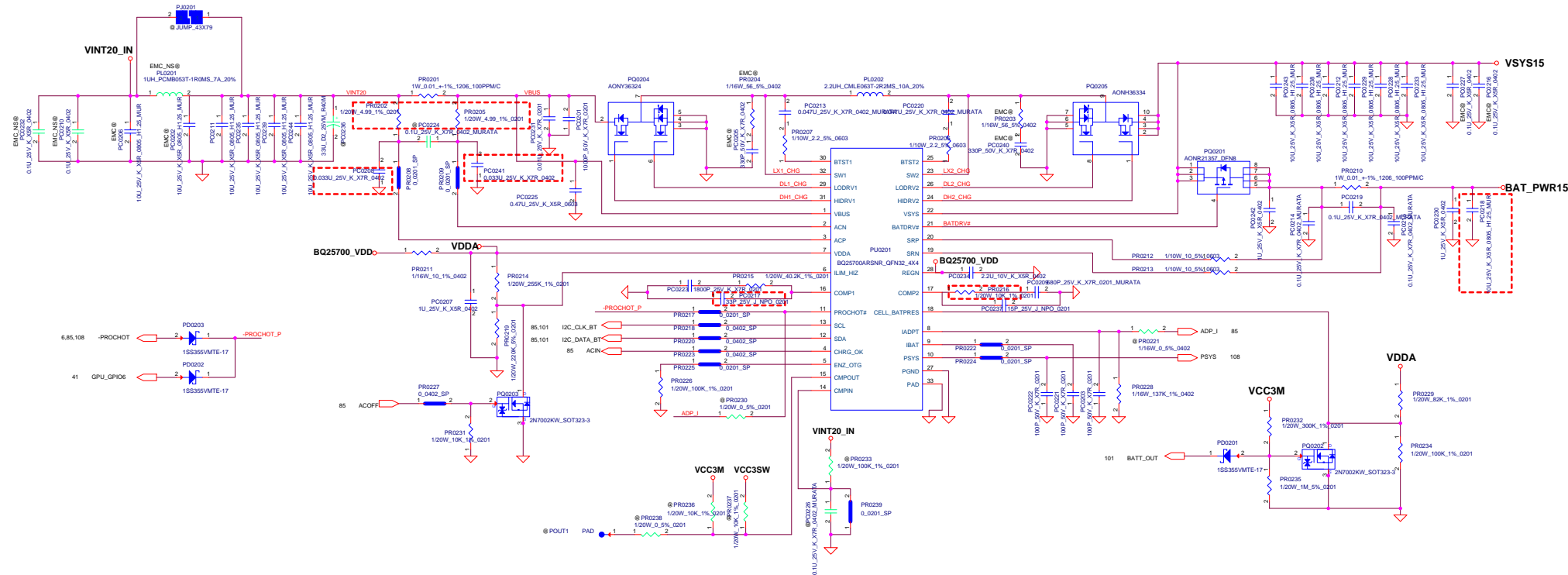
RTC Battery

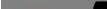


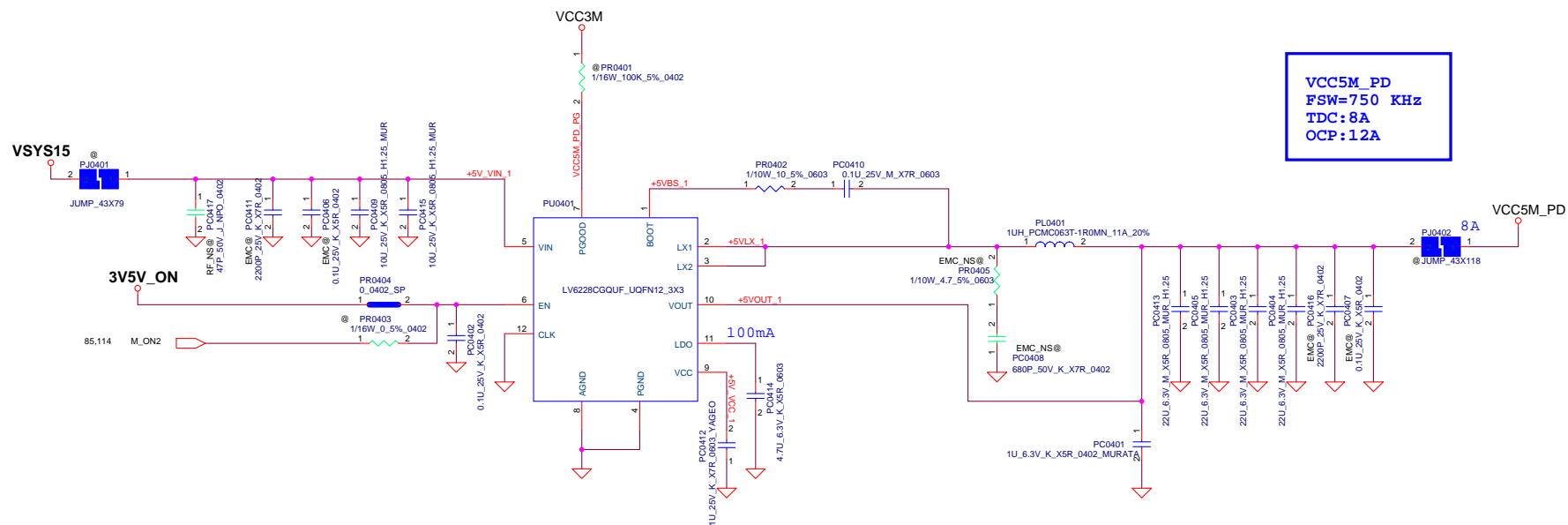
Security Classification		LC Future Center Secret Data		Title				
Issued Date	2013/08/05	Deciphered Date	2014/12/31	VIN Detector				
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				Size	
				Document Number	
				Custom	
				Date	
				GL4A /GL5A NM-C632	
				Tuesday, March 03, 2020	
				Sheet 101 of 129	



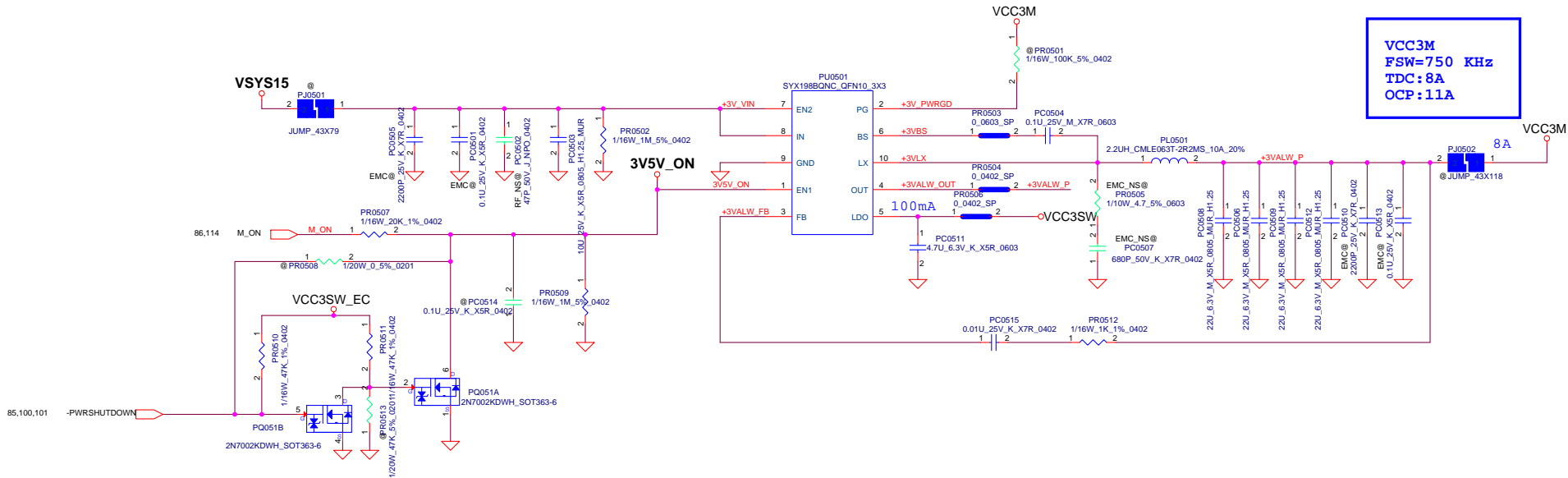
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	DC/DC VCC5M (LV6228)		
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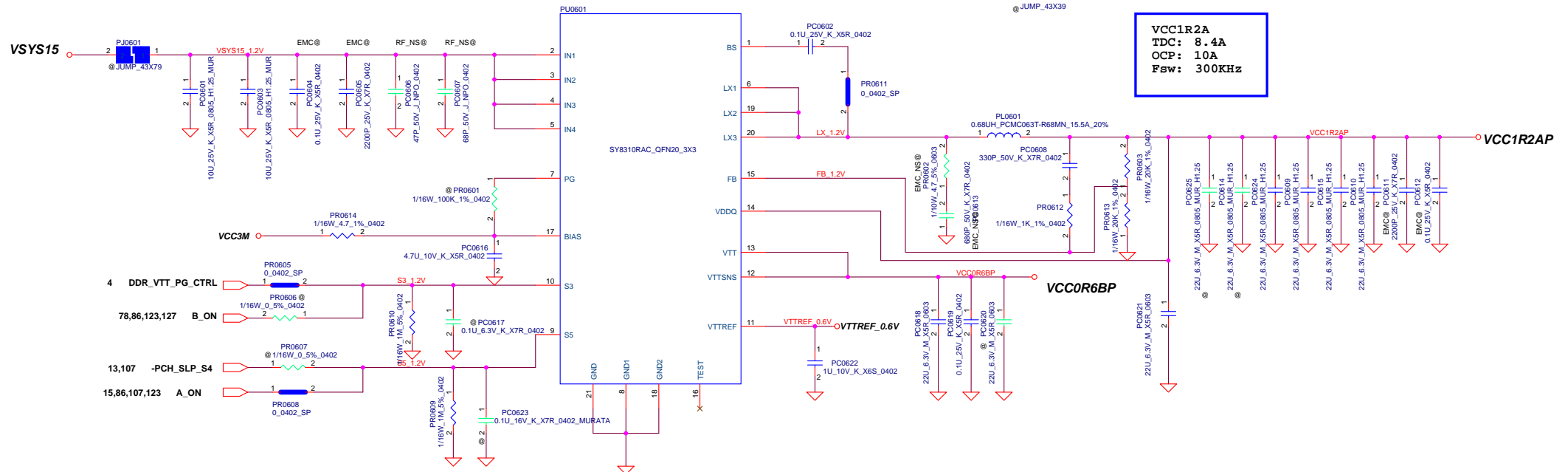
Size Custom	Document Number GL4A /GL5A NM-C632	Rev 2.0
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VSYS15		VSYS15	51,100,102,103,104,106,108,109,110,111,114,118,120
VCC3M		VCC3M	4,11,13,15,16,50,51,59,78,84,85,86,88,102,103,104,106,114,123,124,126,127,128



Security Classification	LC Future Center Secret Data		Title	DC/DC VCC3M (STX198)	Rev 2.0
Issued Date	2013/08/08	Deciphered Date	2013/08/05		
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				Sheet 105 of 129	

VSYS15 VSYS15 51,100,102,103,104,105,108,109,110,111,114,118,120
VCC1R2A VCC1R2A 4,5,15,33,34,35,36
VCC0R6B VCC0R6B 33,34,35,36

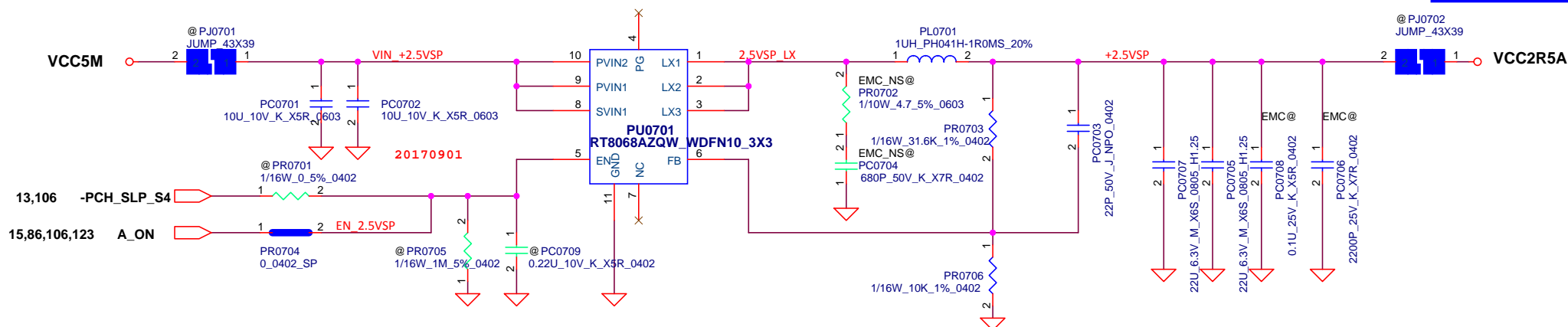


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/05	Deciphered Date	2014/12/31	DC/DC VCC1R2A(RT8231)	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>					
				Size	Document Number
				Custom	GL4A /GL5A NM-C632
				Date:	Tuesday, March 03, 2020
				Sheet	106 of 129

VCC5M 50,51,69,70,84,85,103,108,109,110,111,116,118,123,126,127
VCC2R5A 33,34,35,36

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VCC2R5A
TDC: 2A
OCP: 4A
Fsw: 1MHz

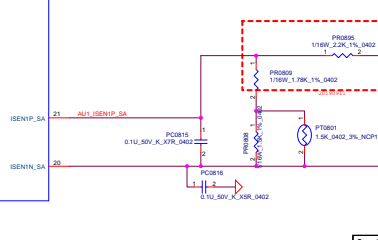
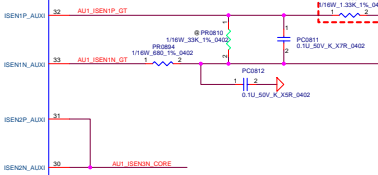
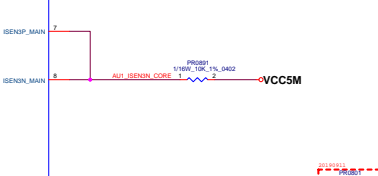
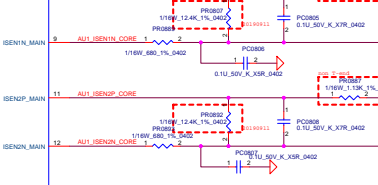
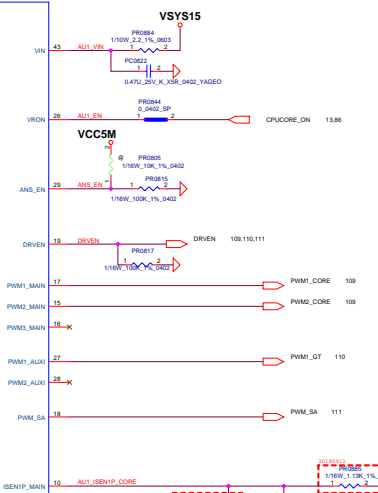
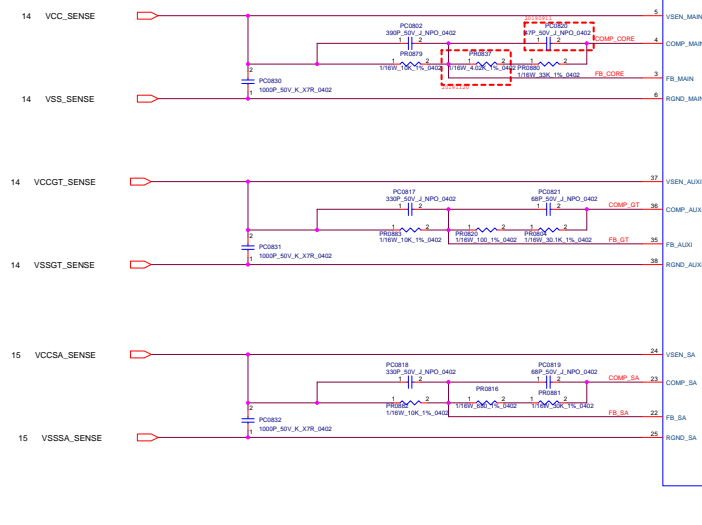
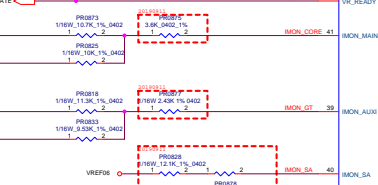
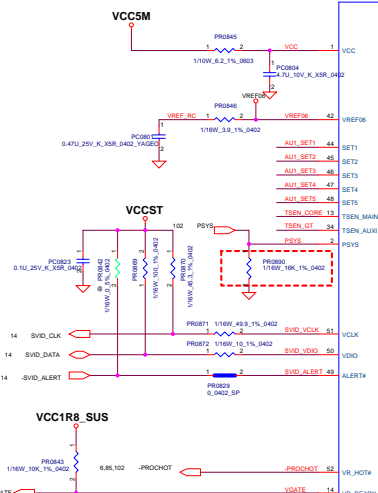
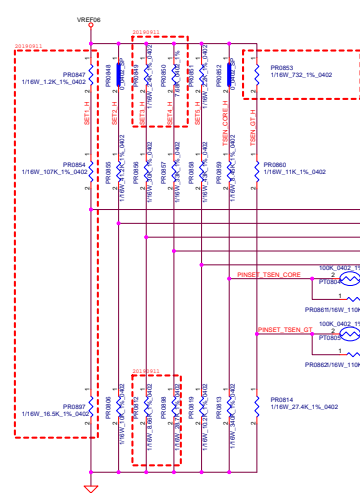


LC Future Center Secret Data				Title	
Security Classification				DC/DC VCC2R5A(RT8068A)	
Issued Date	2013/08/05	Deciphered Date	2014/12/31	Size	Document Number
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				Date:	Tuesday, March 03, 2020
				Sheet	107 of 129

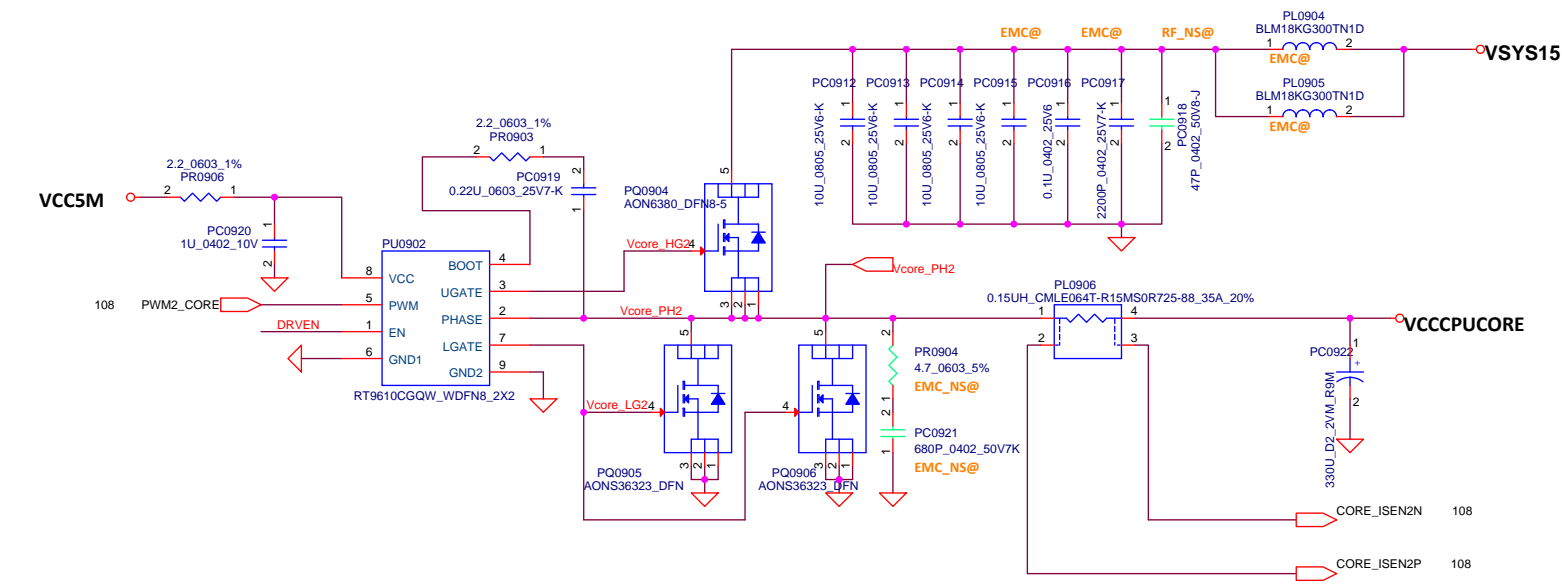
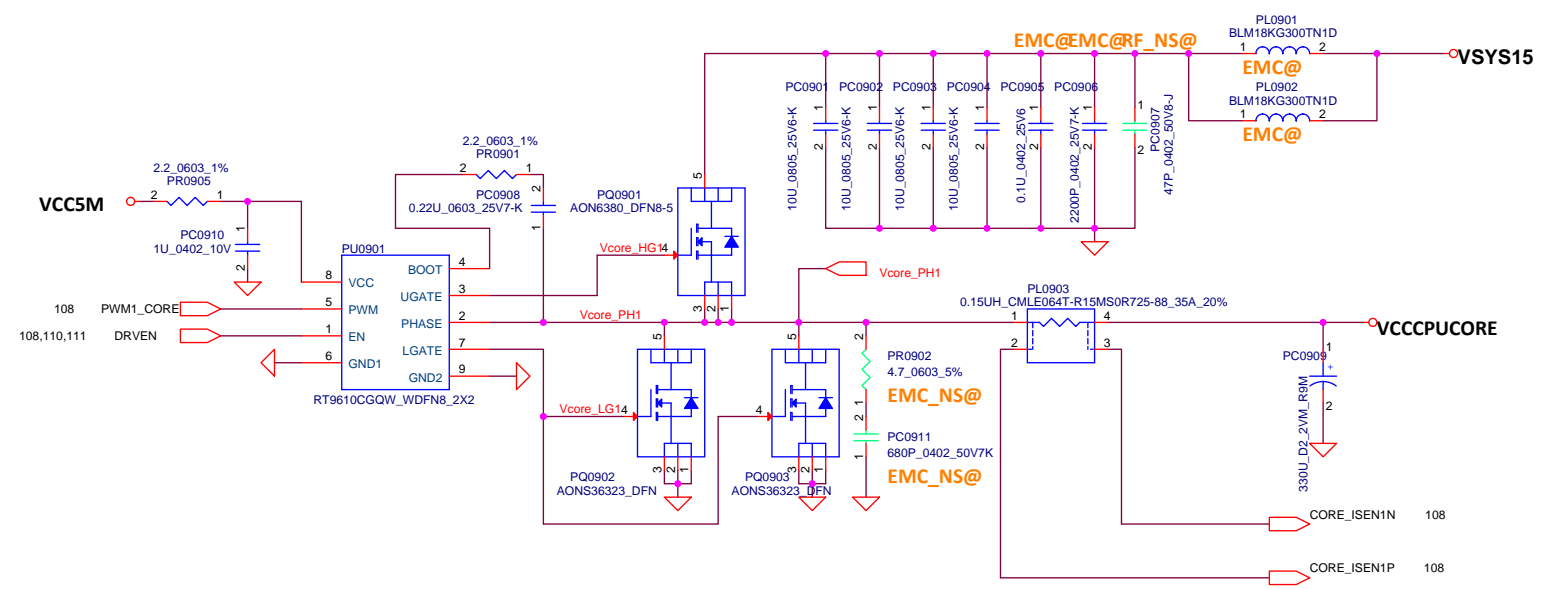


GL4A /GL5A NM-C632

VSYS15 51,100,102,103,104,105,106,108,110,111,114,116,120
VCC5M 50,51,69,70,84,85,103,107,108,110,111,116,118,123,126,127
VCC5T 6,14,15,85,123

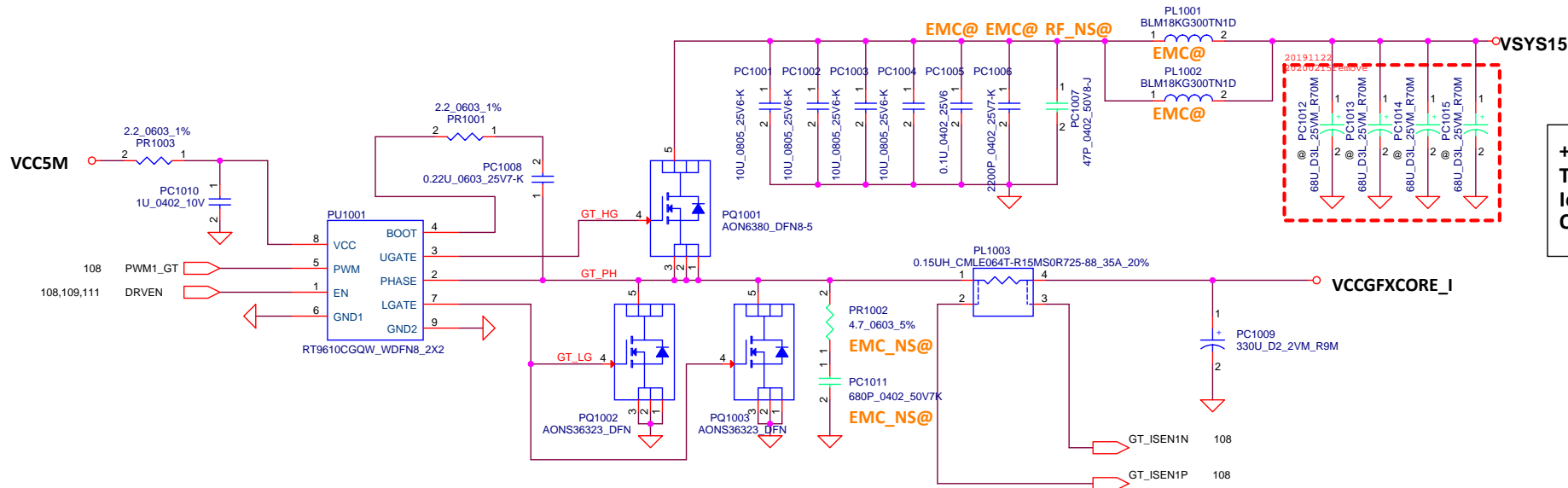


For U42
VCCCPUCORE
TDC= 48A
IccMAX=70A
OCP=76A



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/05	Deciphered Date	2014/12/31	+VCC_CORE	
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				Date:	Tuesday, March 03, 2020
				Sheet	109 of 129

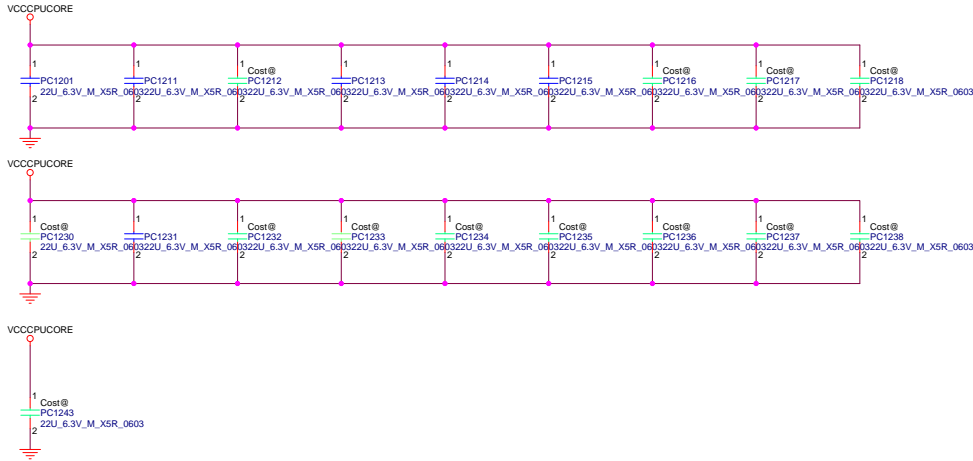
Rev
GL4A /GL5A NM-C632



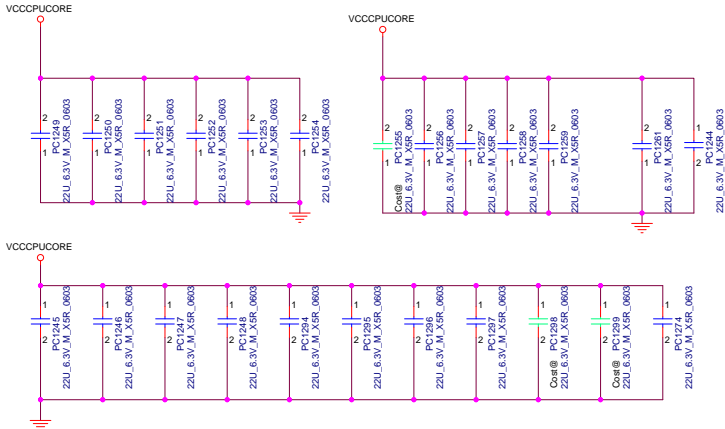
+VCC_GT
 TDC= 22A
 IccMAX=31A
 OCP min = 40A

Security Classification		LC Future Center Secret Data		Title	
Issued Date		2013/08/05		+VCC_GT	
		Deciphered Date		2014/12/31	
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Size Custom		Document Number		Rev	
				GL4A /GL5A NM-C63	
Date:		Tuesday, March 03, 2020		Sheet 110 of 129	

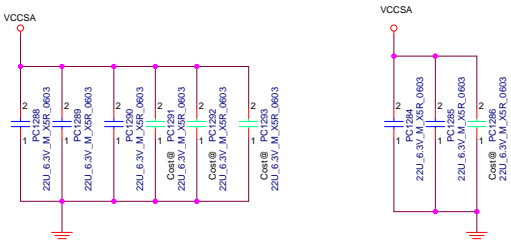
VCCCPUCORE
[Decoupling Requirements for Comet Lake U 4+2 Processor]10uFx8, 47uFx20
Primary side cap.



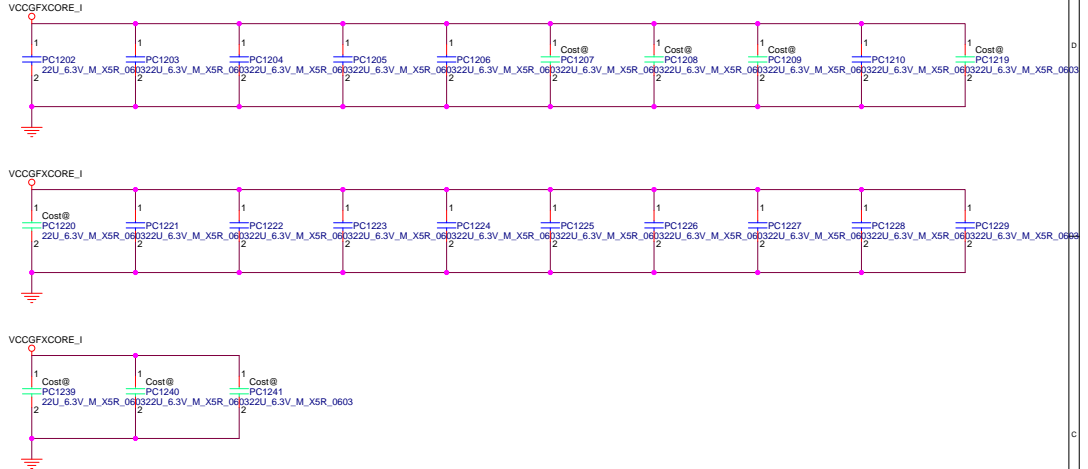
VCCCPUCORE
[Decoupling Requirements for Comet Lake U 4+2 Processor]10uFx8, 47uFx20
Primary side cap.



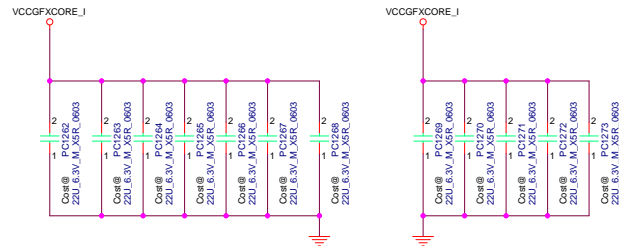
VCCSA
[Decoupling Requirements for Comet Lake U 4+2 Processor]10uFx6, 47uFx2, 10uFx7
Primary side cap.




VCCGFXCORE_I
[Decoupling Requirements for Comet Lake U 4+2 Processor]22uFx15, 47uFx4
Primary side cap.



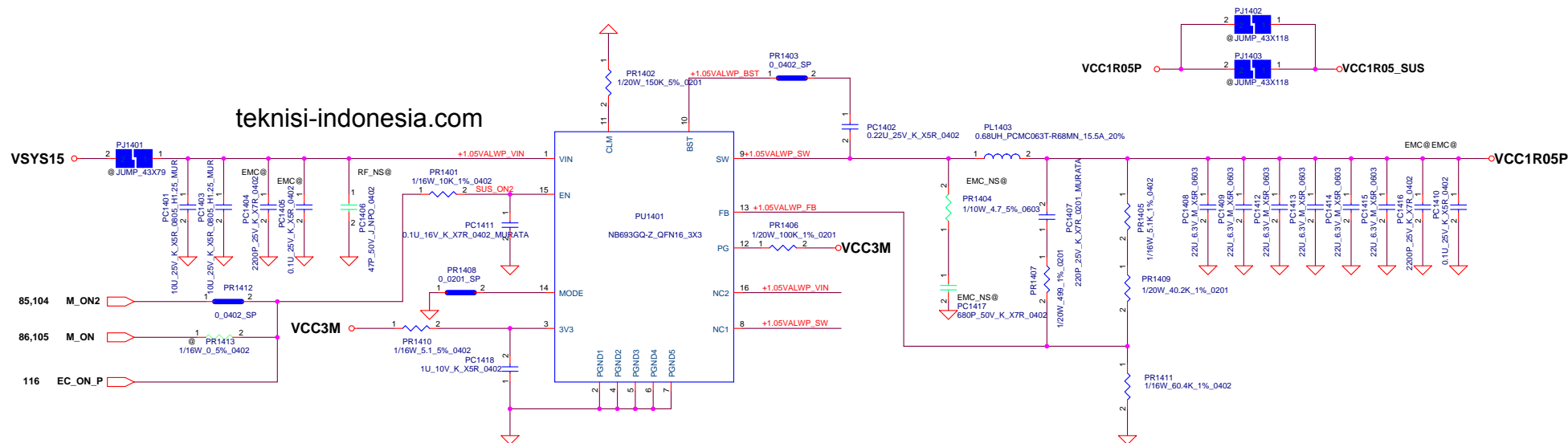
VCCGFXCORE_I
[Decoupling Requirements for Comet Lake U 4+2 Processor]1uFx15, 10uFx15
Secondary side cap.





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				Date: Tuesday, March 03, 2020		Sheet 113 of 128

VCC1R05_SUS
FSW=700KHz
TDC:10A
OCP:13A



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Issued Date	2013/08/05	Deciphered Date	2014/12/31	DC/DC VCC1R05_SUS(NB653)			
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				Date: Tuesday, March 03, 2020		Sheet 114 of 129	

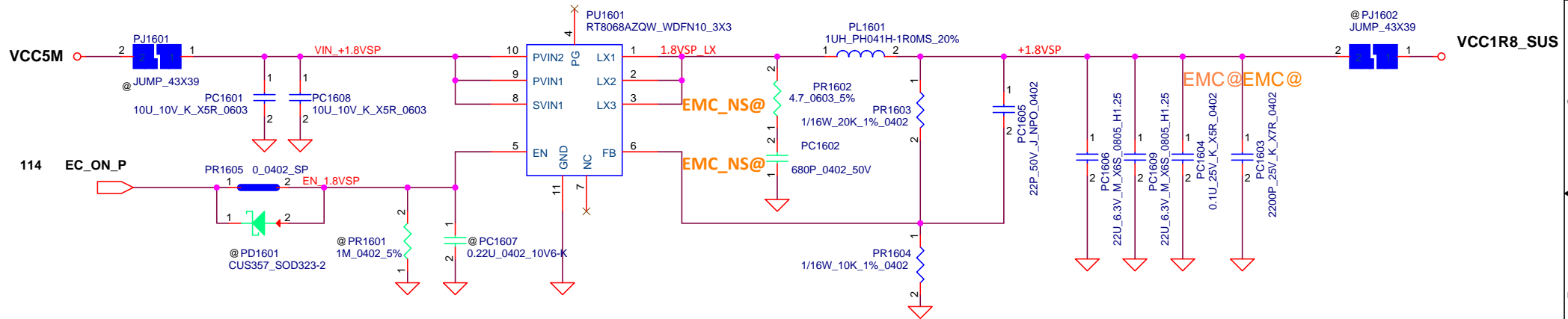
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	BLANK		
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				Date: Tuesday, March 03, 2020		Rev 0.1
				Sheet 115 of 128		

VCC5M 50,51,69,70,84,85,103,107,108,109,110,111,118,123,126,127

VCC1R8_SUS 7,8,16,50,78,85,108


VCC1R8_SUS
TDC: 2A
OCP: 4A
Fsw: 1MHz

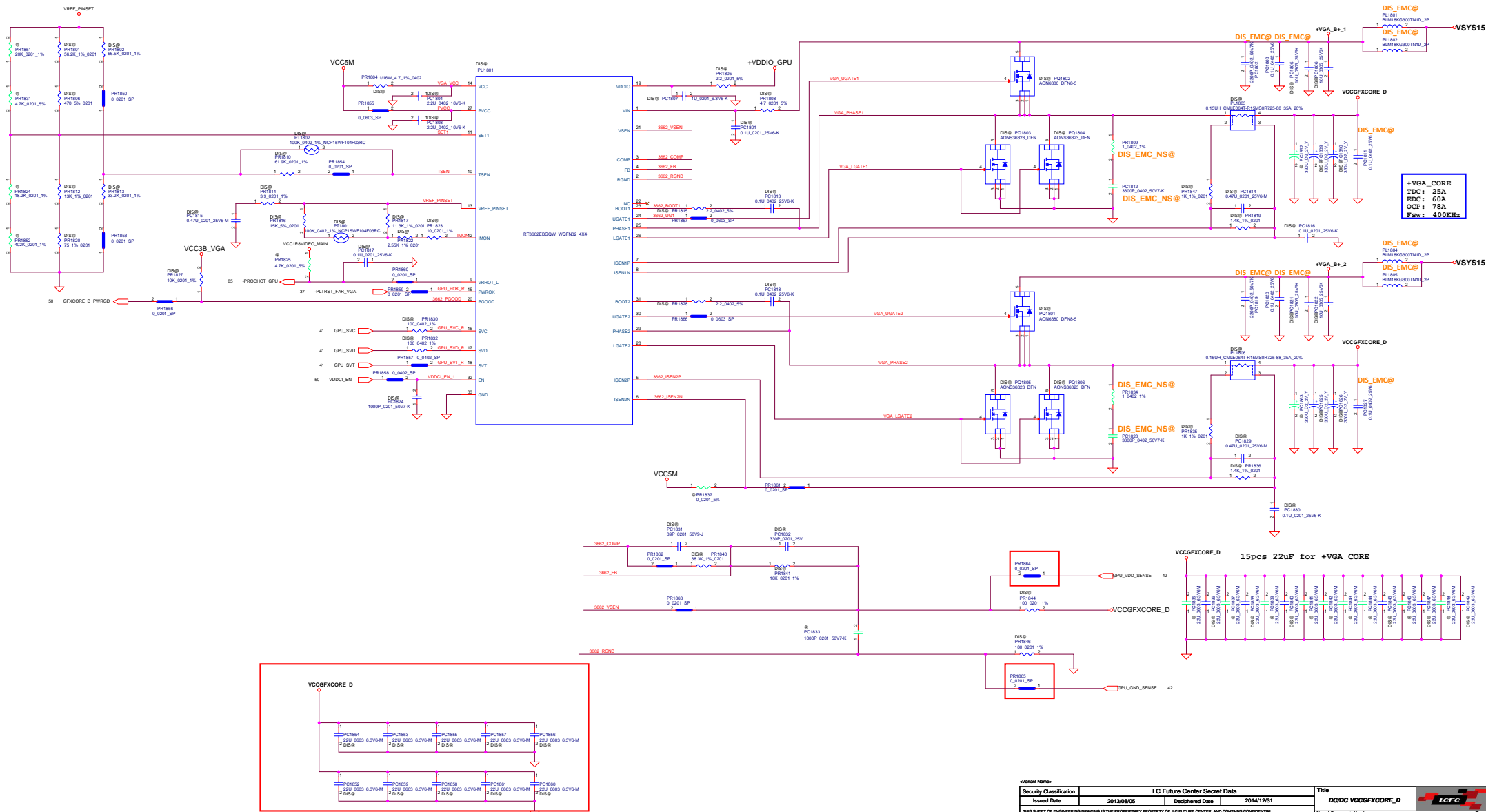


LC Future Center Secret Data				Title	
Security Classification				DC/DC VCC1R8_SUS	
Issued Date	2013/08/05	Deciphered Date	2014/12/31	Size	Document Number
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				Sheet	116 of 129

GL4A /GL5A NM-C632

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				Date: Tuesday, March 03, 2020		Sheet 117 of 128




LC Future Center Secret Data				Title	
Security Classification	Issued Date	Declassified Date	2014/12/31	DODC VCCGFXCORE_D	
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				001	001




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Issued Date	2015/01/12	Deciphered Date	2016/01/12	BLANK		
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				Date: Tuesday, March 03, 2020		Sheet 119 of 128




Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/05	Deciphered Date	2014/12/31	DC/DC VCC1R35VIDEO	
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				Document Number GL4A / GL5A	Rev NM-C632
				Date: Tuesday, March 03, 2020	Sheet 120 of 129

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Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/01/12	Deciphered Date	2016/01/12	BLANK		
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				Date:	Tuesday, March 03, 2020	Rev 1.0
					Sheet	121 of 128

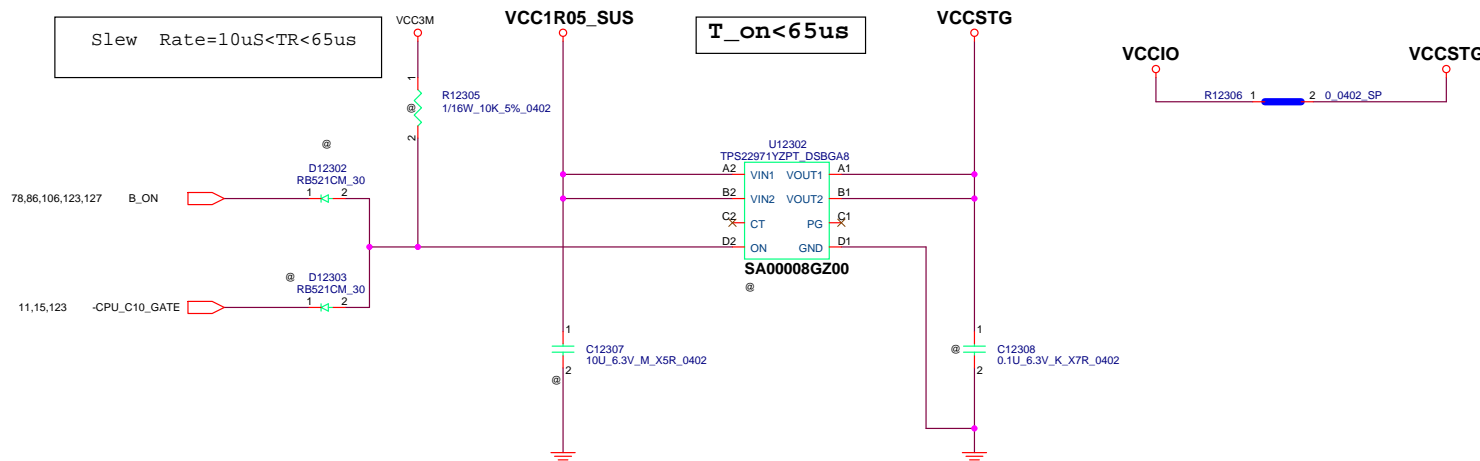
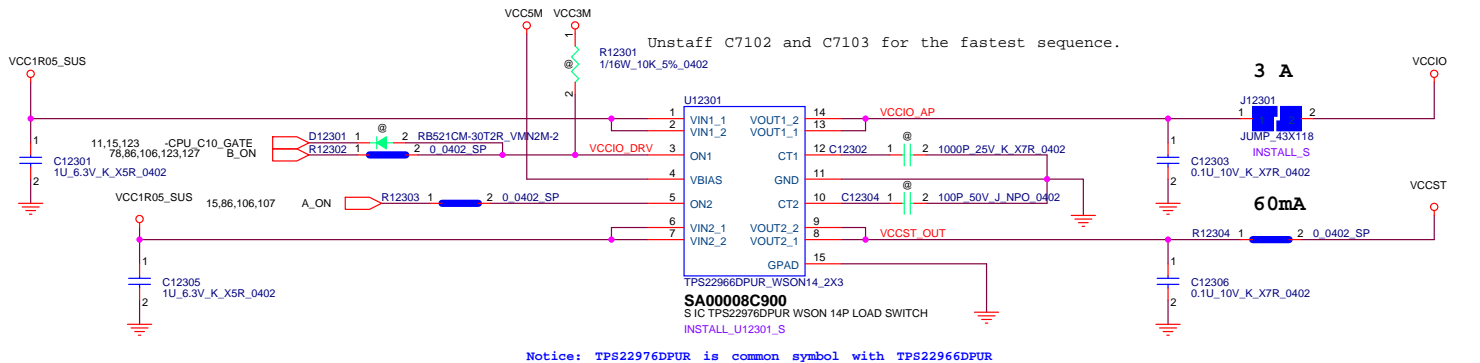
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	BLANK		
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				Date:	Tuesday, March 03, 2020	Rev 1.0
				Sheet		122 of 128

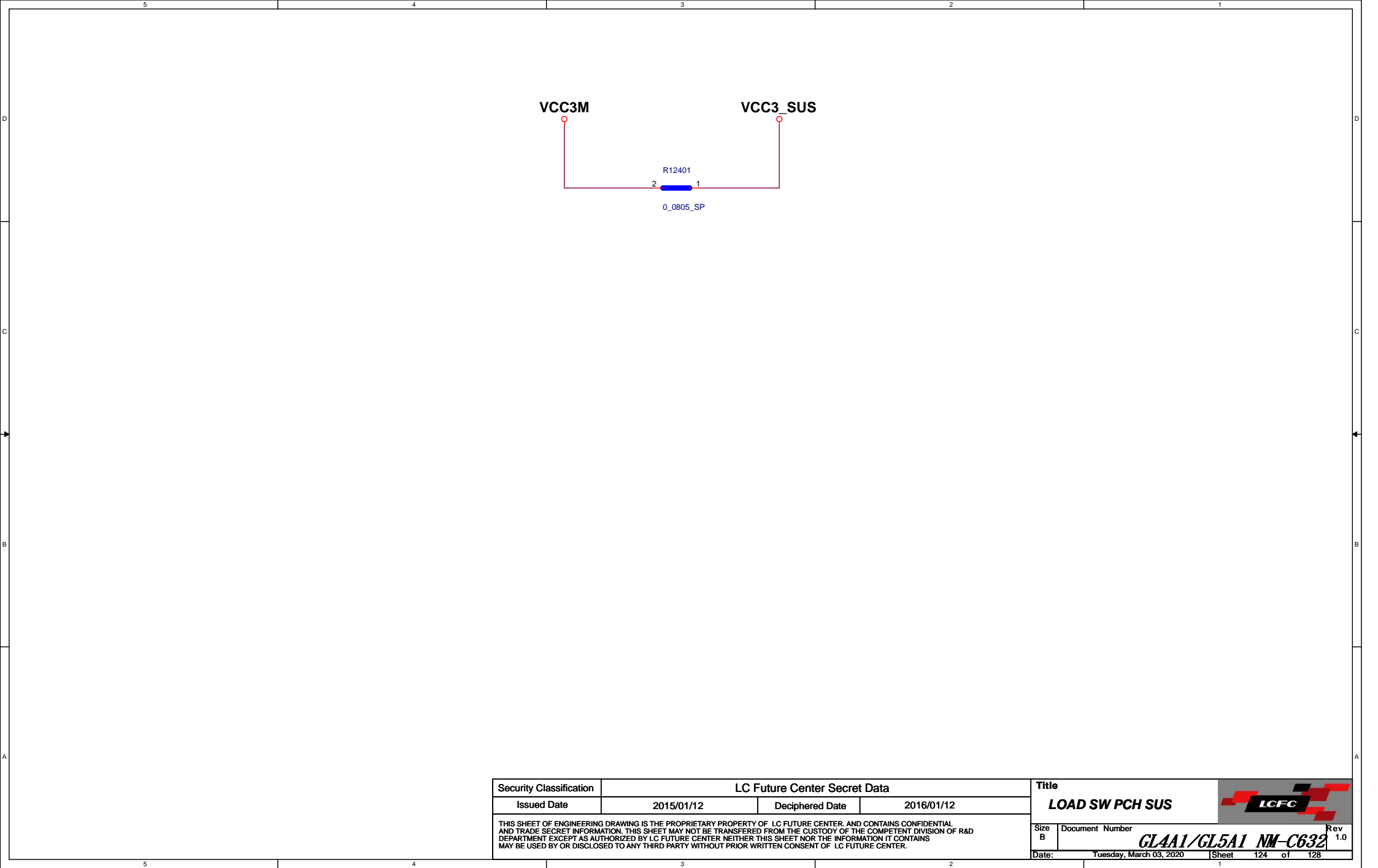
VCC1R05_SUS		VCC1R05_SUS	13,16,50,114
VCCSTG		VCCSTG	6,14,15
VCCIO		VCCIO	3,15,18,85
VCC5M		VCC5M	50,51,69,70,84,85,103,107,108,109,110,111,116,118,126,127
VCCST		VCCST	6,14,15,85,108

TABLE of POWER SWITCH (U12301)		
Vendor	LCFC P/N	Description
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH
GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH
RICHTEK	SA000067200	S IC RT9740AGQW WDFN 14P LOAD SWITCH


VCC1R05M to VCCIO & VCCST



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/01/12	Deciphered Date	2016/01/12	LOADSW VCCIO&VCCST&VCCSTG	
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				Date: Tuesday, March 03, 2020	Rev 1.0



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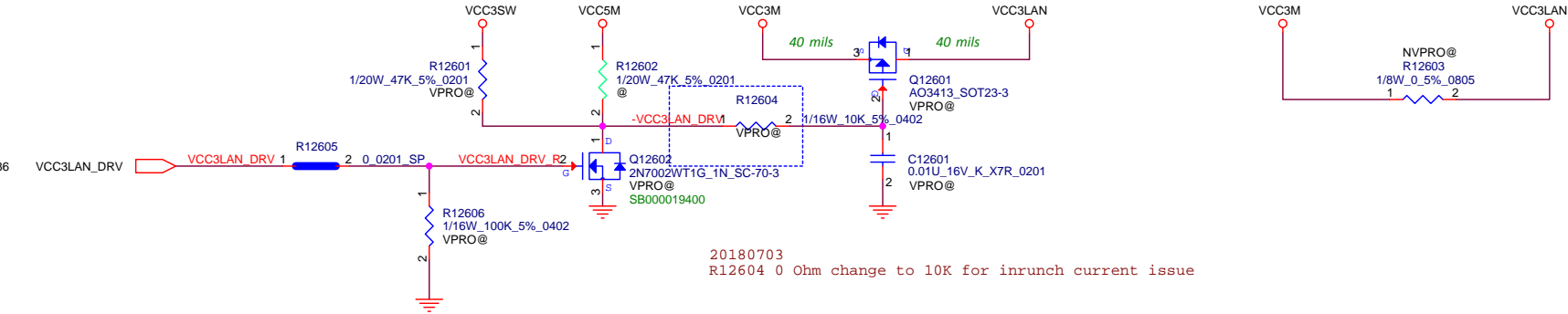
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/01/12	Deciphered Date	2016/01/12	BLANK		
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				Date:	Tuesday, March 03, 2020	Rev 1.0
					Sheet	125 of 128

VCC3LAN VCC3LAN 62,73

Due to solve G3 to S5 wake on lan issue
+3VALW must meet INTEL spec.
Control LAN power sequence must be stuff.

For VPRO

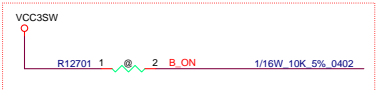
For NVPRO



Security Classification		LC Future Center Secret Data	
Issued Date	2015/01/12	Deciphered Date	2016/01/12
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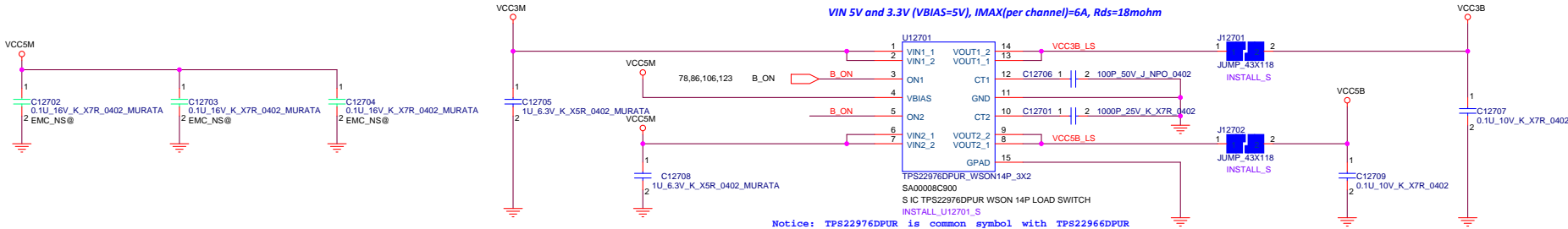
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LOAD SW LAN			
Size B	Document Number	Rev 1.0	
	GL4A1/GL5A1 NM-C632		
Date:	Tuesday, March 03, 2020	Sheet	126 of 128

VCC3SW		VCC3SW	20,51,85,101,102,105,126
VCC3M		VCC3M	4,11,13,15,16,50,51,59,78,84,85,86,88,102,103,104,105,106,114,123,124,126,128
VCC5M		VCC5M	50,51,69,70,84,85,103,107,108,109,110,111,116,118,123,126
VCC5B		VCC5B	51,54,72,78,88,90,96
VCC3B		VCC3B	3,7,8,9,10,12,13,33,35,50,51,64,66,68,70,73,76,78,85,86,88,89,91,92,93,97,98,101



1. MIRROR code, is correct????
2. After reset EC, EC control "Low", not High or Disable.


Smart Switch
VCC5M To VCC5B
VCC3M To VCC3B



Notice: TPS22976DPUR is common symbol with TPS22966DPUR

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TABLE of POWER SWITCH (U12701)		
Vendor	LCFC P/N	Description
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH
GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH
RICHTEK	SA000067200	S IC RT9740AGQW WDFN 14P LOAD SWITCH

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/01/12	Deciphered Date	2016/01/12	LOAD SW B	
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Size	Document Number			GL4A1/GL5A1 NW-C632	Rev
Custom					1.0
Date:	Tuesday, March 03, 2020		Sheet	127	of 128

VCC3WLAN 6,8,66

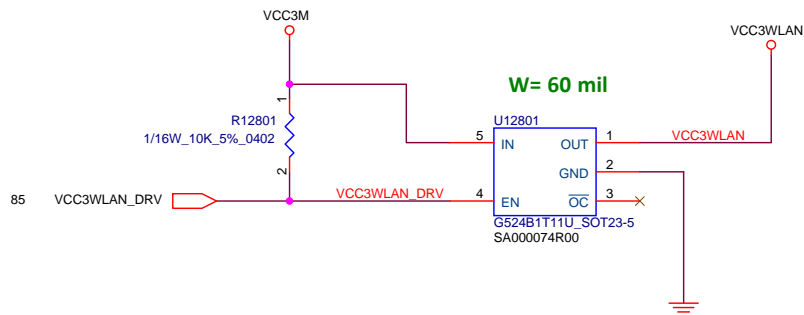
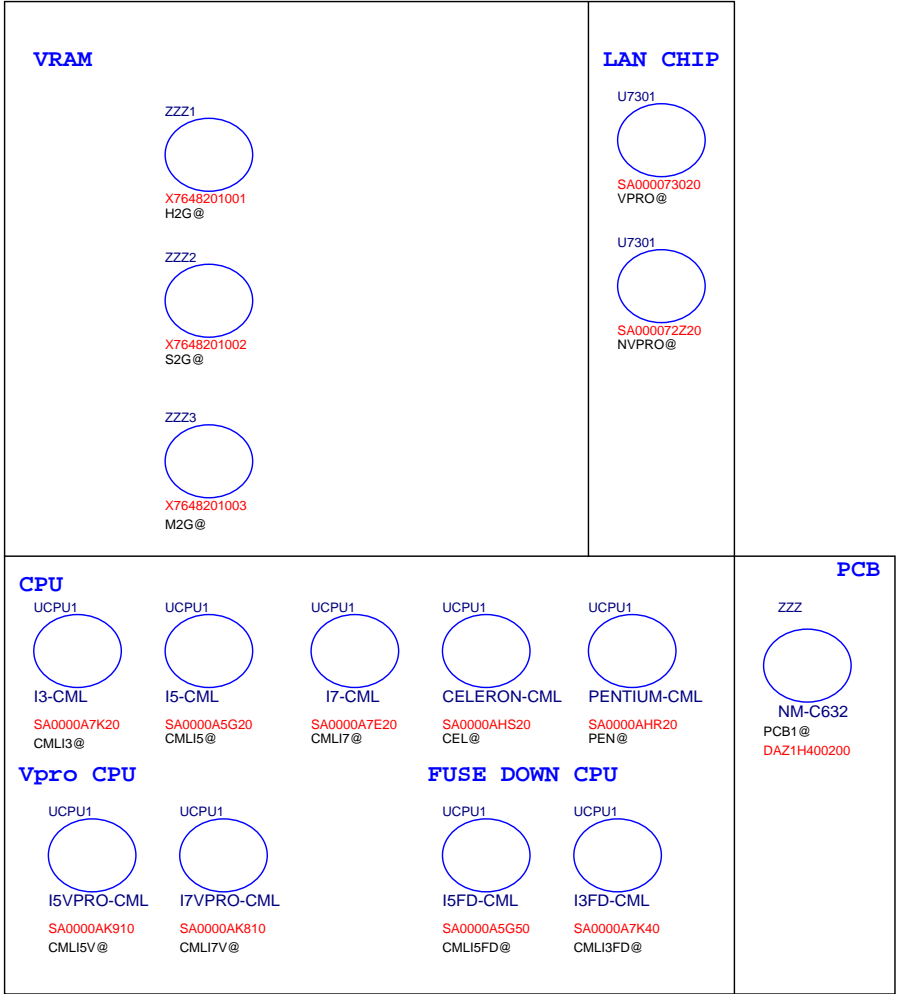



TABLE of POWER SWITCH (U12801)

Vendor	LCFC P/N	Description
GMT	SA000074R00	S IC G524B1T11U SOT23 5P POWER SWITCH
SILERGY	SA000074P00	S IC SY6288C20AAC SOT23 5P POWER SWITCH
RICHTEK	SA0000A2M00	S IC RT9742CGJ5 TSOT-23 5P PWR SW

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/01/12	Deciphered Date	2016/01/12	LOAD SW WLAN	
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